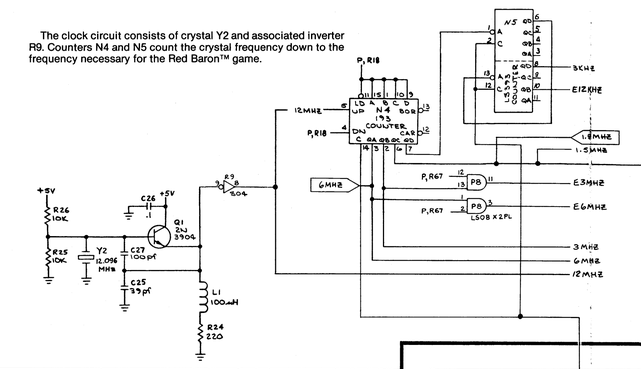
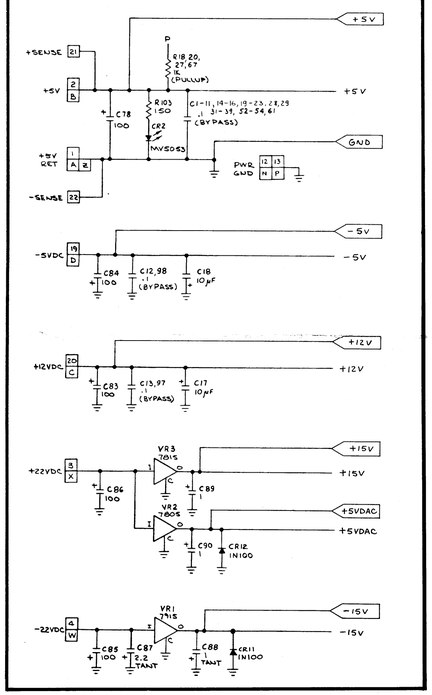
Clock Circiut

The clock circuit consists of crystal Y2 and associated inverter R9. Counters N4 and N5 count the crystal frequency down to the frequency necessary for the Red Baron™ game.



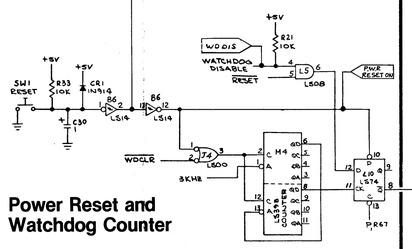
Power Input



Power Reset and Watchdog Counter

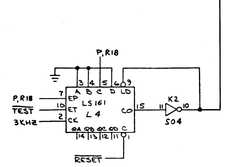
During inital power-up, the delayed charging of capacitor C30 presets flip-flop L10 and clears counter M4. This results in holding RESET input to the MPU low. When the charge of C30 reaches about 1.5 VDC, preset and clear inputs are removed. Counter M4 counts to 128 at 3-KHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter M4 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter M4 will count up to the RESET state and cause the MPU to return to its initialization routine.



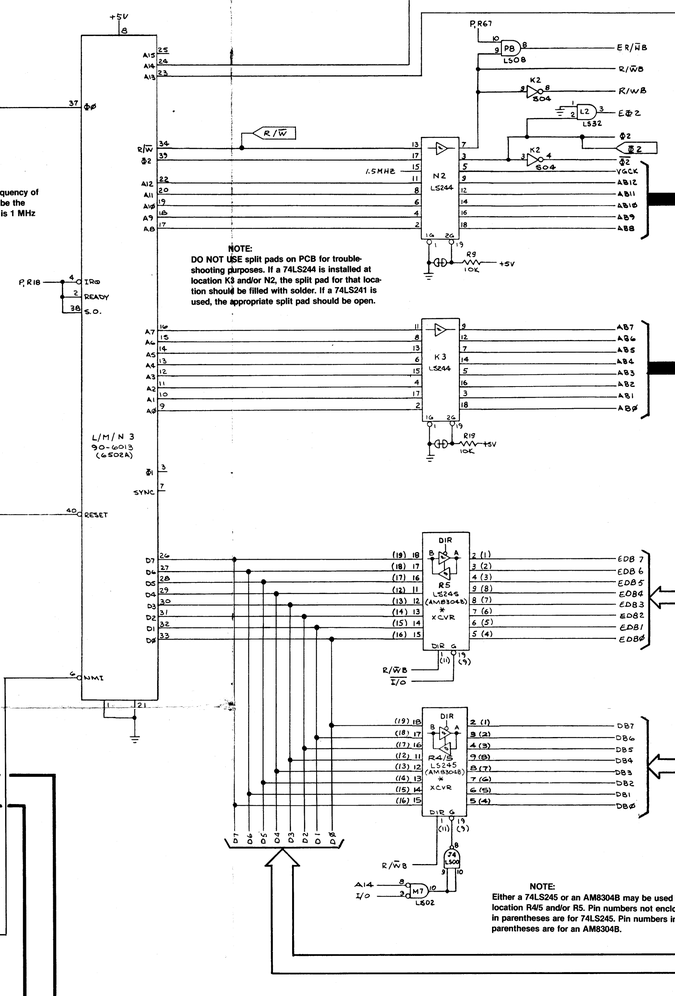
NMI Counter

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter L4. The interrupt occurs when pin 10 of inverter K2 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.



TEST CONNECTOR - FOR ATARI MANUFACTURING ONLY

Microprocessor

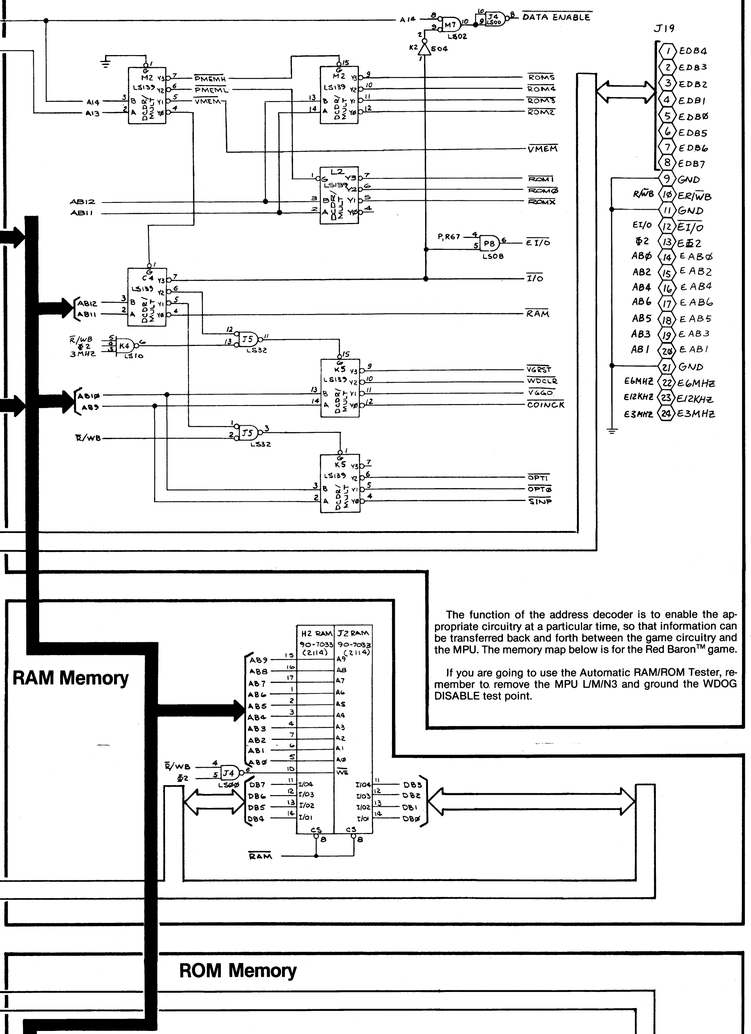


NOTE:
The MPU in this game operates at a frequency of 1.5 MHz. Therefore the MPU chip must be the 6502A. The 6502's maximum frequency is 1 MHz and is not compatible with this game.

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes. If a 74LS244 is installed at location K3 and/or N2, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.

NOTE:
Either a 74LS245 or an AM8304B may be used at location R4/5 and/or R5. Pin numbers not enclosed in parentheses are for 74LS245. Pin numbers in parentheses are for an AM8304B.

Address Decoder

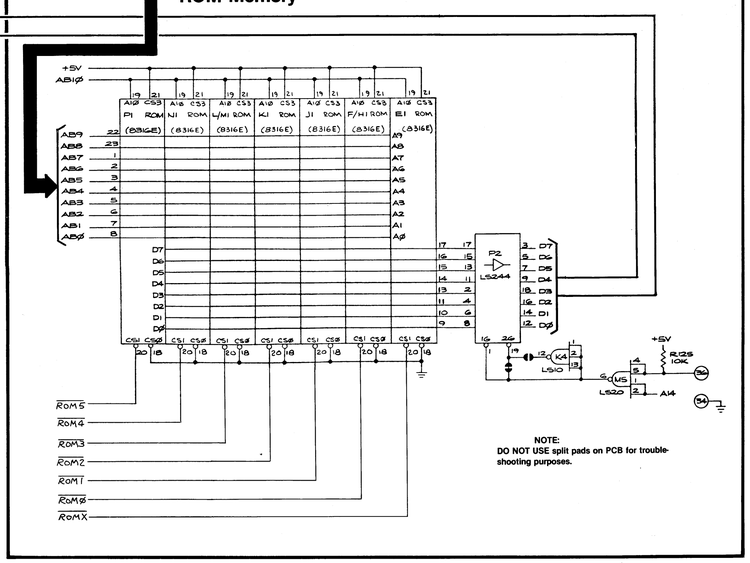


The function of the address decoder is to enable the appropriate circuitry at a particular time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Red Baron™ game.

If you are going to use the Automatic RAM/ROM Tester, remember to remove the MPU L/M/N3 and ground the WDOG DISABLE test point.

RAM Memory

ROM Memory



NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes.

MEMORY MAP

HEXA-DECIMAL ADDRESS	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		D	D	D	D	D	D	D	D	Program RAM (1K)
0800	R								D	Right Coin Switch
	R							D		Center Coin Switch
	R						D			Left Coin Switch
	R					D				Slam Switch
	R				D					Self-Test Switch
	R			D						Diag. Step Switch
	R		D							HALT
	R	D								3 KHz
0A00	R	D	D	D	D	D	D	D	D	Option Switch Inputs
0C00	R	D	D	D	D	D	D	D	D	Option Switch Inputs
1000	W								D	Right Coin Counter
	W							D		Center Coin Counter
	W						D			Left Coin Counter
1200	W									Vector Generator Go
1400	W									Watchdog Clear
1600	W									Vector Generator Reset
1800-187F		D	D	D	D	D	D	D	D	Auxiliary PCB Enable
2000-27FF		D	D	D	D	D	D	D	D	Vector RAM (2K)
2800-2FFF		D	D	D	D	D	D	D	D	Vector RAM/Vector ROM (2K)
3000-3FFF	R	D	D	D	D	D	D	D	D	Vector ROM (4K)
4800-7FFF	R	D	D	D	D	D	D	D	D	Program ROM (14K)

NOTE

- Indicates Edge Connector
- Indicates Interconnect Connector
- Indicates Test Point

ATARI®

Sheet 2, Side A

RED BARON™

Game Microprocessor
Game Address Decoding Circuitry
Analog Vector-Generator PCB Power Input
Clock
NMI Counter
Power Reset and Watchdog Counter
Game Program Memory
Game RAM
Memory Map

Section of 035742-01 & -02 C

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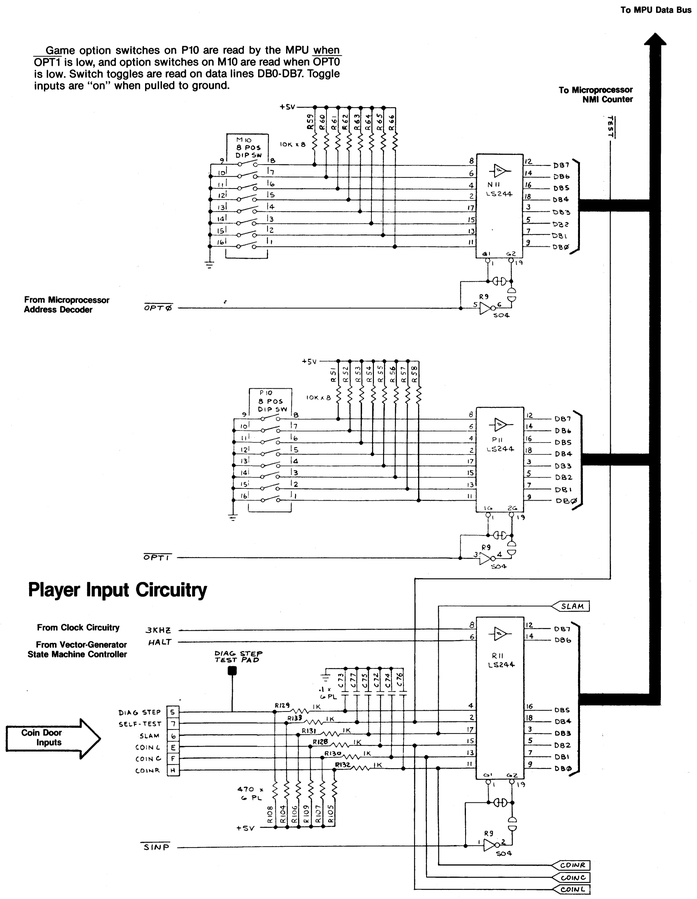
Sheet 2, Side A
DP-171-02 1st printing

Option Switch Inputs

Game option switches on P10 are read by the MPU when $\overline{OPT1}$ is low, and option switches on M10 are read when $\overline{OPT0}$ is low. Switch toggles are read on data lines DB0-DB7. Toggle inputs are "on" when pulled to ground.



Player Input Circuitry

DIAG-STEP (diagnostic step), SELF-TEST, SLAM, COINL, COINC, COINR, 3KHz, and HALT inputs are read by the MPU when $\overline{SINP}$ (switch input) is low. The MPU reads these inputs on data lines DB0-DB7.

DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

ATARI®

Sheet 2, Side B

RED BARON™

Analog Vector-Generator Switch Input
Analog Vector-Generator Video Output
Analog Vector-Generator Coin Counter Output

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Sheet 2, Side B
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Analog Vector Generator PCB Output

The analog vector-generator output circuit consists of the X-axis, Y-axis and Z-axis video-output circuits, and a scaling circuit. The X- and Y-output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample-and-hold circuits and a video-output amplifier. The Z-axis output circuit consists of two input latches, a select multiplexer, and a summation network. The scaling circuit has an input latch, digital-to-analog converter and bias circuit.

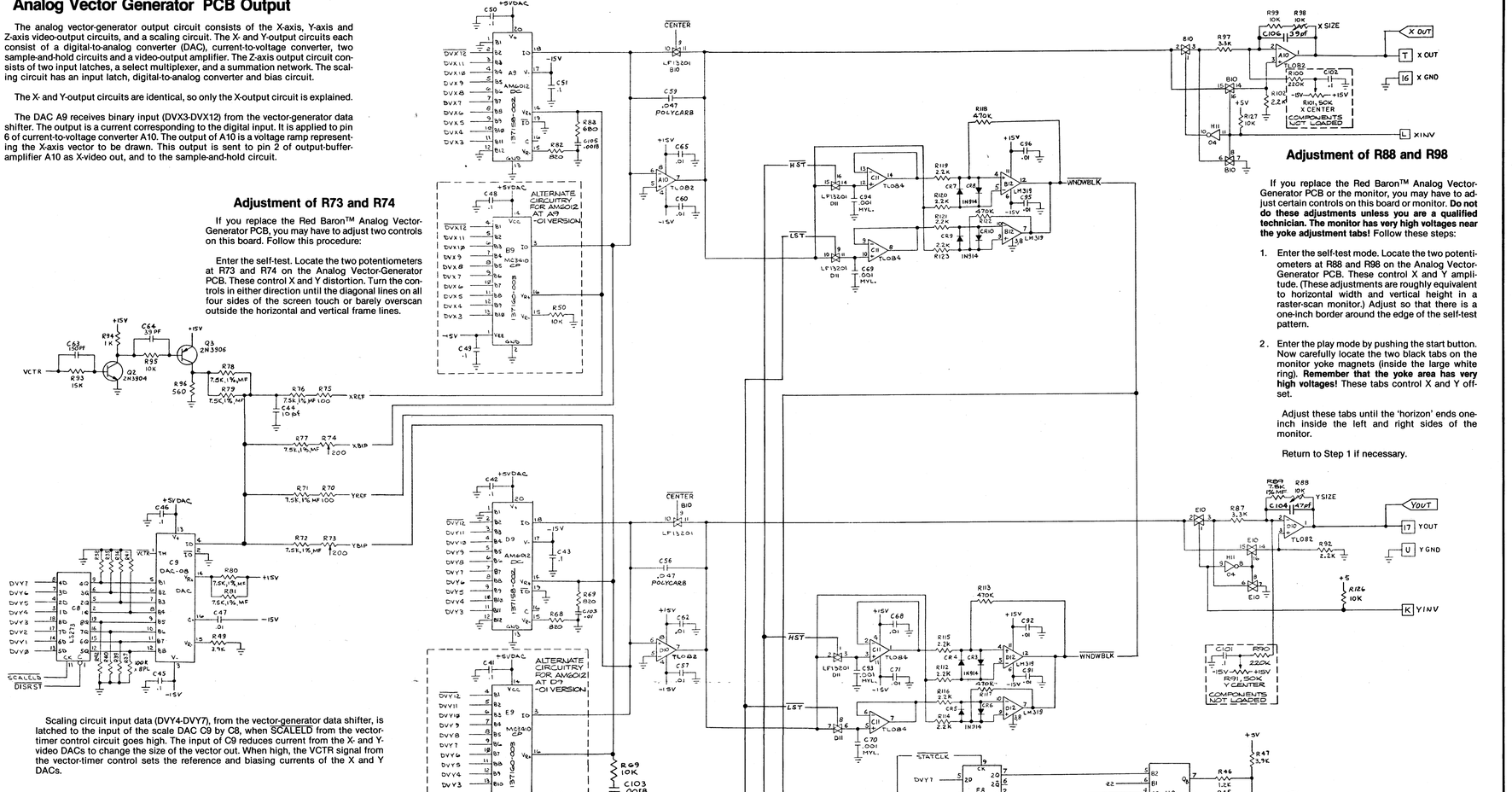
The X- and Y-output circuits are identical, so only the X-output circuit is explained.

The DAC A9 receives binary input (DVX3-DVX12) from the vector-generator data shifter. The output is a current corresponding to the digital input. It is applied to pin 6 of current-to-voltage converter A10. The output of A10 is a voltage ramp representing the X-axis vector to be drawn. This output is sent to pin 2 of output-buffer-amplifier A10 as X-video out, and to the sample-and-hold circuit.

Adjustment of R73 and R74

If you replace the Red Baron™ Analog Vector-Generator PCB, you may have to adjust two controls on this board. Follow this procedure:

Enter the self-test. Locate the two potentiometers at R73 and R74 on the Analog Vector-Generator PCB. These control X and Y distortion. Turn the controls in either direction until the diagonal lines on all four sides of the screen touch or barely overscan outside the horizontal and vertical frame lines.



Adjustment of R88 and R98

If you replace the Red Baron™ Analog Vector-Generator PCB or the monitor, you may have to adjust certain controls on this board or monitor. **Do not do these adjustments unless you are a qualified technician. The monitor has very high voltages near the yoke adjustment tabs!** Follow these steps:

1. Enter the self-test mode. Locate the two potentiometers at R88 and R98 on the Analog Vector-Generator PCB. These control X and Y amplitude. (These adjustments are roughly equivalent to horizontal width and vertical height in a raster-scan monitor.) Adjust so that there is a one-inch border around the edge of the self-test pattern.

2. Enter the play mode by pushing the start button. Now carefully locate the two black tabs on the monitor yoke magnets (inside the large white ring). **Remember that the yoke area has very high voltages!** These tabs control X and Y offset.

   Adjust these tabs until the 'horizon' ends one-inch inside the left and right sides of the monitor.

   Return to Step 1 if necessary.

Scaling circuit input data (DVY4-DVY7), from the vector-generator data shifter, is latched to the input of the scale DAC C9 by C8, when $\overline{SCALELD}$ from the vector-timer control circuit goes high. The input of C9 reduces current from the X- and Y-video DACs to change the size of the vector out. When high, the VCTR signal from the vector-timer control sets the reference and biasing currents of the X and Y DACs.

Window-control latches H10 and J10 receive inputs DVY8 and DVY9 from the vector-generator data shifter. Clocked by $\overline{STATCLK}$ and DVY10, the output will be low-store ($\overline{LST}$), high-store (HST) and $\overline{ZBLANKEN}$. When low, HST and $\overline{LST}$ close the analog switches at D11. Capacitors C69 and C94 charge to a level set by the output voltage ramp at A10 pin 7. When both HST and $\overline{LST}$ are high, D11 opens, and the charge on the capacitors is compared with the output of A10 pin 7 at comparator B12. The output is the x-axis WNDWBLK signal.

Flip-flop F8 receives input data (DVY4-DVY7) from the vector-generator data shifter. This data represents a stored brightness level. When $\overline{STATCLK}$ goes high, the information is passed on to multiplexer H8. The other inputs to H8 are Z0-Z2 from the vector-generator data shifter. This input represents the intensity value of a new vector to be drawn. The output of gate J9 determines which brightness level is used. VCTR, when high, clocks the selected values to the summer circuit R43-R46. The digital output of H8 is converted to a voltage level that represents the intensity of Z out.

Flip-flop C7 and gate D7 make up a brightness-compensation circuit. This circuit takes DVY10-DVY12 from the vector-generator data shifter and clocks it through C7 when GO is high. This digital output is then gated by D7 and is converted to a voltage level. This voltage is summed with the output of H8 so vectors of different lengths appear to be the same brightness.

Shift register P9 controls the blanking of the Z output. Gated by B7, $\overline{ZBLANKEN}$ and $\overline{WNDWBLK}$ produce $\overline{ZBLANK}$. $\overline{ZBLANK}$ and VCTR inputs are shifted to provide a delay. When N9 pin 1 goes high, the Z output is blanked.

Coin Counter Output

This circuit consists of coin counter drivers Q4, Q5, Q6 and data latch M11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high the collector goes low, grounding the return of the coin counter in the coin door.