TABLE OF CONTENTS

SECTION THREE--TESTING THE MEGA

LIST OF ILLUSTRATIONS

SECTION ONE
INTRODUCTION

The Mega 2 and Mega 4 are Motorola MC68000 microprocessor based computers with similar architectures to the 520ST/ 1040ST line. They are styled as a main CPU unit with a detached keyboard. The Mega 2 has 2 megabytes of RAM, the Mega 4 contains 4 megabytes. Both the Mega 2 and Mega 4 have a built-in 1 Megabyte (720K formatted) 3.5 inch floppy disk drive, and an internal switching power supply with built-in cooling fan.

Since the only difference between the Mega 2 and Mega 4 is the size of its RAM, this manual will use ' Mega ' as a generic term which refers to both products.

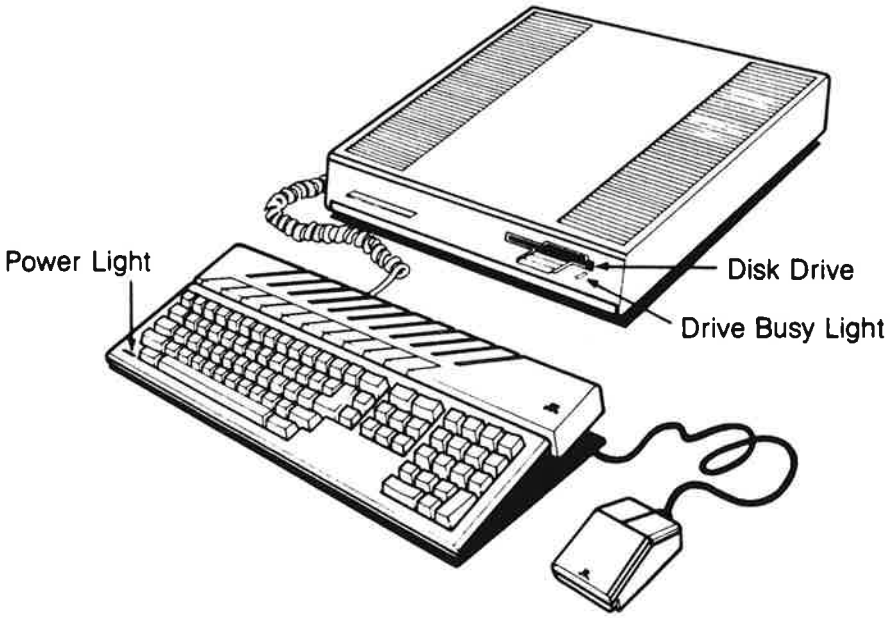


FIG. 1
MEGA COMPUTER SYSTEM

The main components of the Mega 2 and Mega 4 are:

CPU

- Main board assembly
- Disk drive
- Power supply & cooling fan
- RF Shield (upper and lower)
- CPU Plastic case (upper and lower)

KEYBOARD

- Keyboard assembly
- Interface board assembly
- Keyboard Plastics (upper and lower)

MOUSE

- Mouse board assembly
- Mouse Plastics (upper and lower)

CASE DESIGN

Figures 1 thru 4 shows the CPU portion of the MEGA, 5 and 6 shows the keyboard portion, and figure 7 shows the mouse.

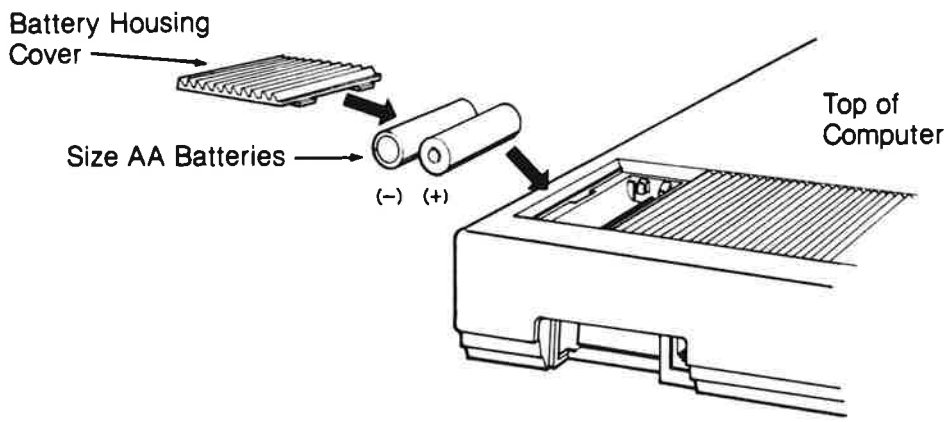


FIG. 2
BATTERY COMPARTMENT

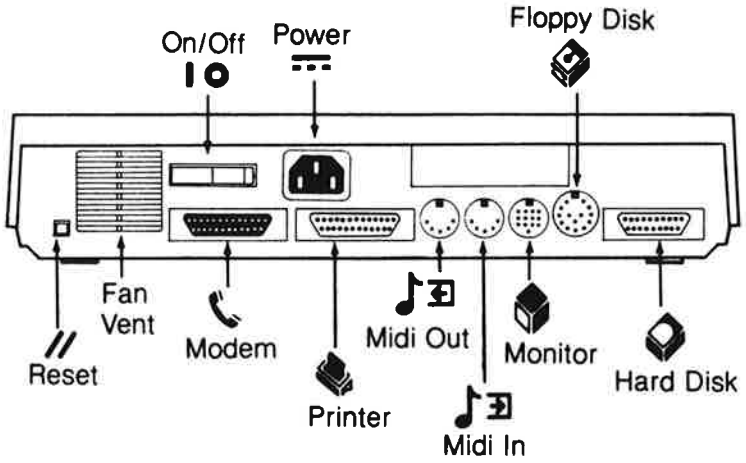


FIG. 3
BACK PANEL

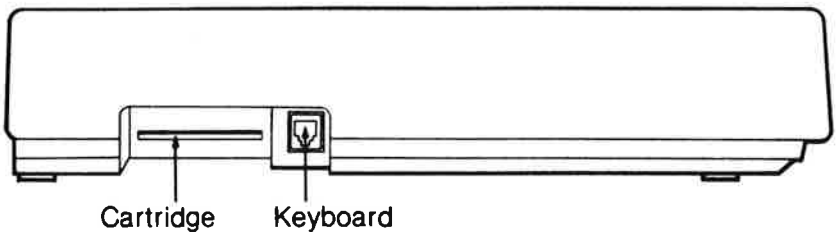


FIG. 4
LEFT SIDE PANEL

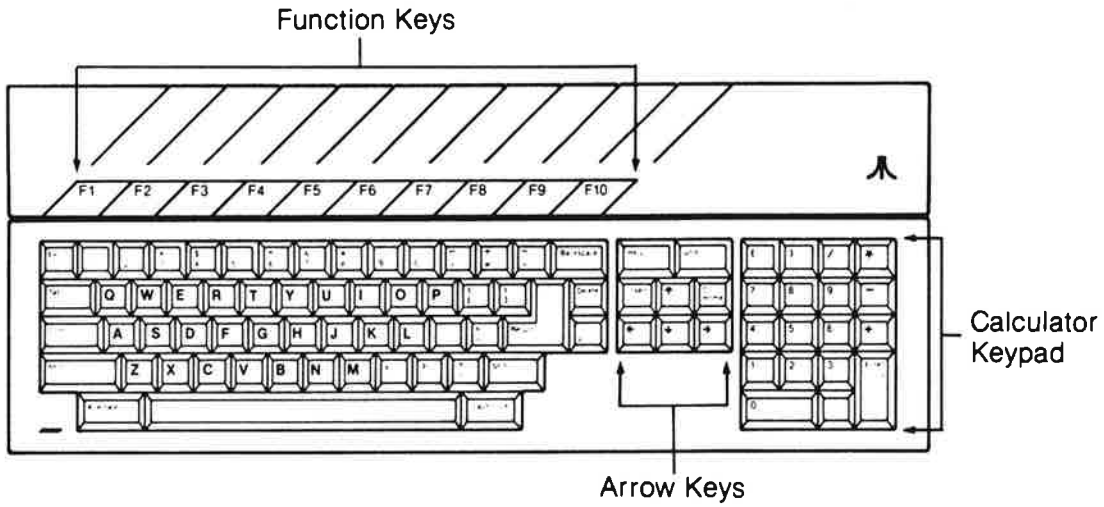


FIG. 5
TOP OF KEYBOARD

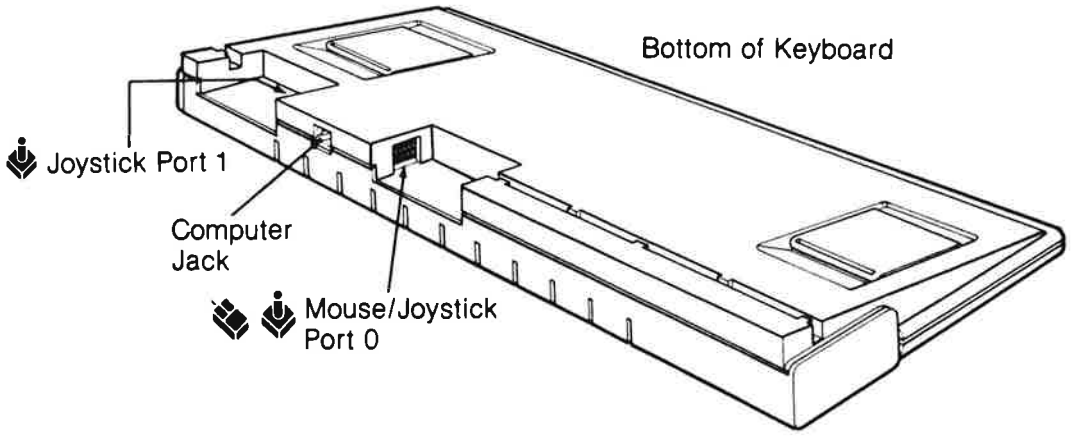


FIG. 5
BOTTOM OF KEYBOARD

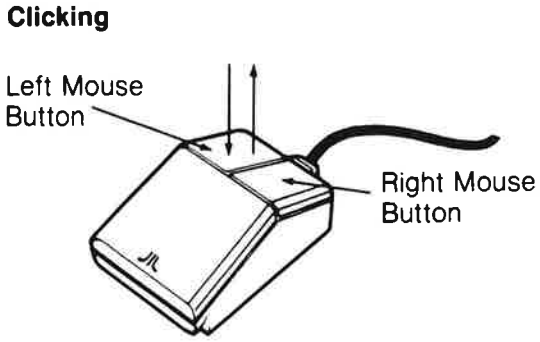


FIG. 7
MEGA MOUSE

Differences from 520ST/1040ST

- New version of TOS
- More memory requiring 74LS243 buffers on MAD lines
- Real time clock chip & support circuit
- Graphics Co-Processor (BITBLiT)
- Internal expansion connector & support circuit
- Cooling fan
- New case styling with detached keyboard

SECTION TWO
THEORY OF OPERATION

OVERVIEW

The Mega 2 and Mega 4 share a common architecture, using the same LSI chip set, and case styling. The only difference is the addition of one bank of 2 Mega-bytes of RAM, for a total of 4 Mega-bytes of RAM on the Mega 4. The hardware can be considered as consisting of a main system (central processing unit and support chips) and several Input/Output subsystems.

Main System

- MC68000 running at 8MHz
- 192 Kbyte Read Only Memory
- 2 or 4 Mega-byte Random Access Memory
- Direct Memory Access support
- System timing and Bus control
- Interrupt control

Audio/Video Subsystem

- Bit Mapped video display, using 32k bytes of RAM, relocatable anywhere in memory. There are three display modes available:
  a. 320 x 200 pixel, 16 color palette from 512 selections
  b. 640 x 200 pixel, 4 color palette from 512 selections
  c. 640 x 400 pixel, monochrome
- BITBLiT support
- Monitor interface analog: RGB, Monochrome
- Audio output: programmable sound chip with 3 voices

Input/Output Subsystems

- Intelligent Keyboard with 2 button mouse/joystick interface
- Parallel printer interface (Centronics)
- RS-232C serial interface
- DMA Port & connector for external drive
- Hard disk drive interface & Laser Printer
- Musical instrument network communication : Musical Instrument Digital Interface (MIDI).
- Real Time Clock with battery backup
- ROM Port

MAIN SYSTEM

The main system includes the microprocessing unit, main memory (ROM and RAM), system control, interrupt control, and general purpose DMA controller.

Microprocessing Unit

The Mega uses the Motorola MC68000 16 bit external/32 bit internal data bus, 24 bit address bus microprocessor, running at 8 MHz.

Glue

Glue (named because it holds the system together) is such an important component that it is involved in nearly every operation in the computer. The functions may be summarized as follows:

Clock dividers-- takes the 8 MHz clock and outputs 2 MHz and 500 KHz clocks.

Video timing-- Blank, DE (Display Enable), Vsync, and Hsync are used to generate signals for the video display. There is a Read/Write register in Glue which may be written to configure for 50 or 60 Hz operation (done by the Operating System).

Interrupt priority-- interrupts from the MFP and video timing are coded into four levels of priority on outputs IP11 and IPL2 to the 68000. These levels correspond to no interrupts, MFP interrupts, VSYNC interrupt, HSYNC interrupt.

Signal and Bus arbitration-- Glue decodes addresses to generate chip selects to the 6850s, MFP, DMA Controller, Programmable Sound Generator, Memory Controller, and ROMs. It receives signals from the MFP, DMA, Memory Controller, to synchronize data transfer. It arbitrates the bus during DMA transfers to prevent CPU and DMA devices from interfering with each other (see DMA below).

Illegal condition detection--Glue asserts Bus Error (BERR) if certain conditions are violated, such as writing to ROM, writing byte sized data to a word sized register, or writing to system memory when the processor is in user mode. Also occurs if a device does not respond within the required time limit. For example, the CPU tries to read from memory and the Memory Controller does not assert DTACK.

Main Memory

Main memory consists of 192 kbytes of ROM and one or two banks (2 Mega-byte each) of dynamic RAM. In addition, the cartridge slot allows access to 128 Kbytes of ROM. All memory is directly addressable. The components of the memory system are: ROM, RAM, RAM buffers, Memory Controller, and Glue. The Operating System resides mostly in ROM, with optional segments loaded from disk into RAM.

RAM is organized as 16 bit words and may be accessed 16 bits at a time or 8 bits at a time. Even numbered addresses refer to the high 8 bits of a word and odd addresses refer to the low 8 bits. RAM is made up of 1 Megabit X 1 chips; in the Mega 2 there are 16 chips, giving 2 Mbytes, while in the Mega 4 there is an additional bank of 16 chips, giving two times the memory, or 4 Mbytes.

RAM memory map:

000008-000800	System memory (priveliged access)
000800-1FFFFF	low bank
200000-3FFFFF	high bank (Mega 4 only)

Note: the first 8 bytes of ROM are mapped into addresses 0-7. These are reset vectors which the 68000 uses on start-up.

The Operating System is located in two 1Meg x 8 ROM chips in current versions (192k).

Memory Controller--takes addresses from the address bus and converts to Row Address Strobe (RAS) and Column Address Strobe (CAS). All RAM accesses are controlled by this Atari proprietary chip, which is programmable for up to 4 Megabytes of memory. The Operating System determines how much memory is present and programs the Memory Controller at power-up. The Memory Controller refreshes the dynamic RAMs, loads the Video Shifter with display data, and gives or receives data during direct memory access (DMA).

Glue--decodes addresses for RAM and ROM and asserts output signals to enable these devices (also decodes addresses for most hardware registers to provide chip selects, as well as many other functions. See Glue description above.).

Direct Memory Access

Direct memory access is provided to support both low speed (250 to 500 Kilobits/sec) and high speed (up to 8 Megabits/sec) 8bit device controllers. The floppy disks transfer data via low speed DMA and the hard disk (or other devices on the hard disk port) transfer at high speed. For DMA to take place, the Memory Controller is given the address of where to take data from or put data in RAM, the DMA Controller is set up (which channel, high speed or low speed, and how many bytes) and the peripheral is given a command to send or receive data. The entire block of data (the size must be given to the DMA Controller and the peripheral before the operation starts) is then transferred to or from memory without intervention by the CPU.

For example, in a transfer of a sector from the floppy to memory, the floppy controller will signal the DMA Controller that a byte is ready by asserting FDRQ, the DMA chip will read the byte and signal Glue, Glue will signal the Memory Controller, and the Memory Controller will read the byte from the DMA Controller and place it in the address which was set up previously. The DMA Controller will then wait for the next byte from the floppy controller, and the process will repeat until the specified number of bytes has been transferred. Transfers from memory to floppy are similar. The floppy initiates every transfer by requesting data on FDRQ.

At high speed (hard disk port), there is a difference: as a byte is ready to transfer to or from the DMA chip, the DMA Controller will assert ACK to let the peripheral know the byte is available or has been read. The DMA Controller can store up to 32 bytes in internal memory. This is necessary if the 68000 is using the bus, and the DMA must wait to transfer to memory. Data may be input from the port without being lost or slowing down the transfer speed.

MFP Interrupt Control

The 68901 MFP handles up to 16 interrupts. Currently all but one are used. Each interrupt can be masked off or disabled by programming the MFP. The 8 inputs are also directly readable by the CPU. When the MFP receives an interrupt input, or generates an interrupt internally, if the interrupt is enabled, MFPINT will be driven low. When the CPU is ready to respond, it signals interrupt acknowledge (FC0-2 high and VMA low) and Glue will assert IACK (interrupt acknowledge). The MFP will assert DTACK and put a vector number on the data bus, which the CPU will read and use to calculate the address of the interrupt routine.

The interrupts controlled by the MFP are: monochrome monitor detect (MONOMON), RS232 (including CTS, DCD, RI), disk (FDINT and HDINT), parallel port BUSY, display enable (DE, equals start of display line), 6850 IRQs for keyboard and MIDI data, and MFP timers.

Not all I/O operations use interrupts. The CPU can also poll the MFP while waiting for an operation to complete. The MFP has four timers, used by the Operating System for event timing and used by the RS232 port for transmit and receive clocks.

AUDIO/VIDEO SUBSYSTEM

The video subsystem consists of the video display memory, the Memory Controller, Glue, a graphics control chip (Video Shifter), a graphics processing unit (BITBLiT), and a discrete section to drive the video output. The audio subsystem consists of a Programmable Sound Generator chip with a transistor output amplifier.

Video Shifter

There are 16 color palette registers in the shifter. All 16 are may be used in low resolution, 4 may be used in high resolution, and only one is used in high resolution (actually, only bit 0 of register 0 is used for inverse/normal video). Each palette is programmed for 8 levels of intensity of red, blue, and green, so there are 8 x 8 x 8 = 512 colors possible. For a given pixel, the color which is displayed is taken from the palette referred to by getting information from each logical plane (see description of video display memory below). The shifter will output the red, green, and blue levels specified by that palette; note there are three outputs for each color. Each output is either on or off. Thus, the number of possible output levels is 2 to the 3rd power = 8. The three outputs are summed through a resistor network to proportion the voltage level to give 8 equal steps. In monochrome mode, the color palettes are bypassed and there is a separate output.

Video Display Memory

Display memory is part of main memory with the physical screen origin located at the top left corner of the screen. Display memory is configured as 1, 2, or 4 (high, medium, or low resolution) logical planes interwoven by 16 bit words into contiguous memory to form one 32 Kilobyte physical plane starting at a 256 byte half page boundary. The starting address of display memory is placed in the Memory Controller's Video Base Address register by the Operating System or application. The Memory Controller will load display information into the Video Shifter 16 bits at a time, and the Video Shifter will decode this information to generate a serial display stream. In monochrome mode, each bit represents 1 pixel on or off. In color, bits are combined from each plane to generate the correct level of red, green, and blue.

For example, in low resolution (4 planes) 4 words are loaded into the Video Shifter for each word (16 pixels displayed on the screen. The Video Shifter combines bit 0 from each word to form a four bit number (0-15), and takes the color from the palette referenced by that number (e.g. 0101=5, use color from palette register 5) and outputs those levels, then takes bit 1 from each plane and outputs the color from the palette referenced by those four bits, etc.

Glue

Glue provides timing control to the Memory Controller, video output, and monitor/RF output. VSYNC input to the Memory Controller causes the starting address of the display memory to be reloaded into the address counter during vertical blanking. DISPLAY ENABLE (DE) tells the Memory Controller and Video Shifter that a display line is being scanned and data should be loaded into the Video Shifter. BLANK shuts off the video output from the Video Shifter during periods when the scan is not in a displayable part of the screen. VSYNC and HSYNC both go to the monitor output and RF modulator. These signals synchronize the monitor or T.V. vertical and horizontal sweep to the display signal.

Memory Controller

In addition to the inputs from Glue mentioned above, there are two output control signals associated with video. DCYC strobes data from display memory into the Video Shifter. CMPCS (color map select) is active only when changing the color attributes in the color palettes.

Sound Synthesizer

The YM2149 Programmable Sound Generator (PSG) produces music synthesis, sound effects, and audio feedback (e.g. alarms and key clicks). The clock input is 2 MHz; the frequency response range is 30 Hz to 125 KHz. There are three sound channels output from the chip, which are mixed and sent to the monitor speaker.

The PSG is also used in the system for various I/O functions relating to printer port, disk drive, and RS232.

Atari Blitter

This is a DMA device that moves block of memory data from a source location to a destination location through a given logic operation. Single or multiple word increments and decrements are provided for transfer to destination. There are 16 possible logic operation rules associated with the merging of source and destination data. In addition, with the 16 word patterns ram and three 16 bit end-mask registers, the blit can also be used to perform operations such as area seed filling, pattern filling, brush line drawing, text and graphic transformations, etc.

For more information, please refer to the user manual which is included in the Developer Kit.

Real Time Clock with Battery Backup

This device has counters for Time and Calendar built-in. Clock data are expressed with BCD code. The lower four address and data lines are used to program the device and access the clock through signal lines RTCCS, RTCRD, RTCWR which generated from a decoder. A RESET line is also provided to reset the chip when the system is reset. The main clock supplied to the device is a 32.768 Khz oscillator which will be adjusted by a trimmer condenser so that it will output through the CLKOUT line a standard clock signal of 16.384 Khz. In addition, a 3V battery backup can be used to keep the clock running during power down.

For more detail, please refer to the application manual from the manufacturer (RICOH part number RP5C15)

Video Interface

The two types of interface are provided in the Megas are analog RGB and monochrome. The presence of a monochrome monitor is detected by the MONOMON input (when a monochrome monitor is connected, it will be low). The possible displays are:

Monochrome: single emitter follower amplifier driving the output of the Video Shifter.

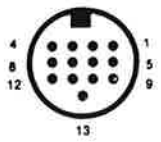
RGB: resistor network sums outputs for each color. The three colors each have an emitter follower amplifier to drive output.

Monitor Inputs:

Hsync--TTL level, negative, 3.3 k ohm.
Vsync--TTL level, negative, 3.3 k ohm.
Monochrome--digital 1.0V P-P, 75 ohm.
R,G,B--analog 0-1.0V P-P, 75 ohm.
Audio--1V. P-P, 1k ohm.

Monitor

1 — Audio Out
2 — Composite Sync
3 — General Purpose Output
4 — Monochrome Detect
5 — Audio In
6 — Green
7 — Red
8 — Plus 12-Volt Pullup
9 — Horizontal Sync



10 — Blue
11 — Monochrome
12 — Vertical Sync
13 — Ground

FIG. 8
MONITOR PORT

Musical Instrument Communication

The Musical Instrument Digital Interface (MIDI) allows the integration of the Mega with music sysnthesizers, sequencers, drum boxes and other devices possessing MIDI interfaces. High speed (31.25 Kilobaud) asynchronous current loop serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port). MIDI specifies that data consist of 8 data bits preceded by one start bit and followed by one stop bit.

Communication takes place via a 6850 ACIA. The CPU reads and writes to the 6850 in response to interrupts which are passed from the 6850 to the MFP interrupt controller. The system is interfaced to the outside via two inverters on the transmit side and an LED/photo-transistor chip on the input side. The input signal is routed around through two inverters to the output connector where it is called MIDI THRU in order to allow chaining of multiple devices on the MIDI bus.

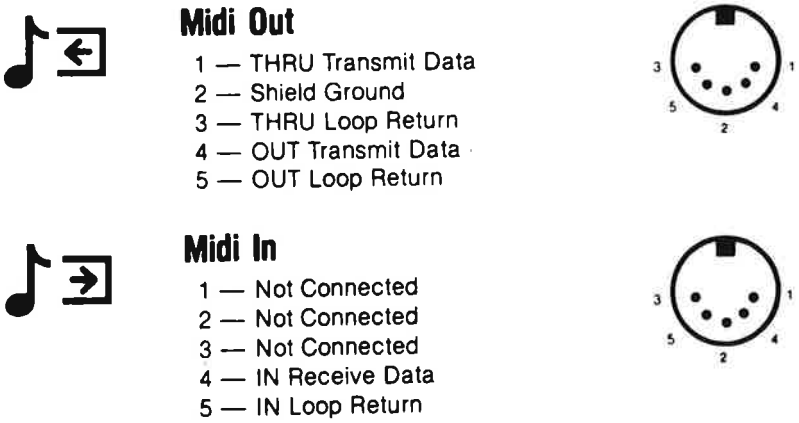


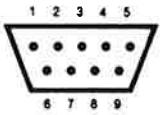
FIG. 9
MIDI PORTS

Intelligent Keyboard

The keyboard transmits make/break key scan codes, ASCII codes, mouse data, joystick data, in response to external events, and time-of-day data (year, month, day, hour, minute, second) in response to requests by the CPU. Communication is controlled on the main board by a 6850 device and on the keyboard assembly by the 1MHz 8 bit HD6301 Microcomputer Unit. The HD6301 has internal RAM and ROM. Included in ROM are self-test diagnostics which are performed at power-up and whenever the RESET command is sent over the serial communication line by the CPU. The MC6850 is read and written to by the CPU in response to interrupts which are passed to the CPU by the MFP interrupt controller.

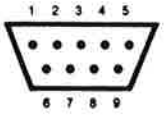
The 2 Button Mouse is an opto-mechanical device with the following characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second and a maximum pulse phase error of 50 percent. The joystick/mouse port has inputs for up, down, left, right, right button, left button. The right button equals the joystick trigger, and the left button is wired to the second joystick port trigger. The joystick has four directions (up, down, etc.) and one trigger.

Mouse / Joystick



1 — Up/XB
2 — Down/XA
3 — Left/YA
4 — Right/YB
5 — Not Connected
6 — Fire/Left Button
7 — + 5VDC
8 — Ground
9 — Joy1 Fire/Right Button

Joystick



1 — Up
2 — Down
3 — Left
4 — Right
5 — Reserved
6 — Fire Button
7 — + 5VDC
8 — Ground
9 — Not Connected

FIG. 10
MOUSE/JOY PORT

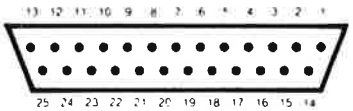
Parallel Interface

The parallel port is primarily intended as a Centronics type printer interface, but can also be used as a general purpose I/O port. Centronics STROBE and BUSY are supported. BUSY is read by the MFP chip. Data and strobe signals are output by the YM2149 PSG chip. Not all Centronics printers are compatible with this port. The current loading on the data lines should not exceed 2.3 mA. (This corresponds to a 2.2k ohm resistor pull-up on the printer side.)

The port can be programmed to be input or output. The PSG chip is read directly by the CPU, with Glue doing address decode to provide chip select.

Printer

1 — STROBE Output
2 — Data 0
3 — Data 1
4 — Data 2
5 — Data 3
6 — Data 4
7 — Data 5
8 — Data 6
9 — Data 7



10 — Not Connected
11 — BUSY Input
12-17 — Not Connected
18-25 — Ground

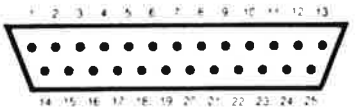
FIG. 11
PRINTER PORT

RS232C Interface

The RS232C interface provides asynchronous serial communication with five handshake control signals: Request to Send and Data Terminal Ready are output by the PSG chip; Clear to Send, Data Carrier Detect, and Ring Detect are input to the MFP chip. The MFP contains a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) which handles data transmission and reception. The 2.4576 MHz clock to the MFP is divided by the timer D (pin 16) output of the MFP to provide the basic clock for receiver and transmitter. Data rate of 50 to 19200 bits per second are supported. 1488 line drivers and 1489 line receivers with +/- 12v. supply meet the EIA RS232C standard for electrical interface.

Modem

1 — Protective Ground
2 — Transmitted Data
3 — Received Data
4 — Request to Send
5 — Clear to Send
6 — Not Connected
7 — Signal Ground
8 — Data Carrier Repeat
9-19 — Not Connected



20 — Data Terminal Ready
21 — Not Connected
22 — Ring Indicator
23-25 — Not Connected

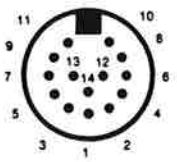
FIG. 12
RS232 PORT

Disk Drive Interface

The Mega computers have a built-in floppy disk controller (a Western Digital 1772) and logic for selecting up to two single or double sided drives. The Mega has one built-in floppy disk drive and provision for one external disk drive. The Western Digital WD1772 Controller services both drives. Drive and side selection is done by outputs on the YM2149 PSG chip. The CPU reads and writes to the 1772 through the DMA Controller. The 1772 interrupts the CPU on the INTR line, via the MFP interrupt controller. The 1772 accepts high level commands, such as seek, format track, write sector, read sector, etc. and passes data to the DMA Controller (see DMA controller under Main System, above, for details on DMA transfer). The 1772 interrupts the CPU when the operation is complete. The CPU is freed from much of the overhead of disk I/O.

Floppy Disk

1 — Read Data
2 — Side 0 Select
3 — Logic Ground
4 — Index Pulse
5 — Drive 0 Select
6 — Drive 1 Select
7 — Logic Ground
8 — Motor On
9 — Direction In
10 — Step



11 — Write Data
12 — Write Gate
13 — Track 00
14 — Write Protect

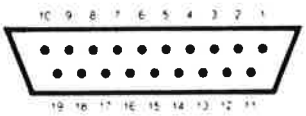
FIG. 13
EXTERNAL FLOPPY PORT

DMA Port; Hard Disk Interface

The hard disk drive interface is provided through the DMA controller; the hard disk controller is off-board and is board and is sent commands via an SCSI-like (Small Computer System Interface) command parameter block. Data is transferred via DMA. Writing to the external controller causes HDCS (Hard Disk Chip Select) to go low and CA1 to go high. DMA transfers are controlled by the external device. When data is available, or the device is ready to accept data, HDRQ will be driven high by the external controller. The DMA chip must respond within 250 nanoseconds with ACK (low) to acknowledge that data is on the bus or has been read from the bus. The Memory Controller feeds data to or accepts data from the DMA Controller. Transfers can take place at up to 1 Mbyte/second.

Hard Disk

1 — Data 0
2 — Data 1
3 — Data 2
4 — Data 3
5 — Data 4
6 — Data 5
7 — Data 6
8 — Data 7
9 — Chip Select
10 — Interrupt Request
11 — Ground
12 — Reset



13 — Ground
14 — Acknowledge
15 — Ground
16 — A1
17 — Ground
18 — Read/Write
19 — Data Request

FIG. 14
EXTERNAL HARD DISK PORT

SYSTEM STARTUP

After a RESET (power-up or reset button) the 68000 will start executing at the address pointed to by locations 4-7, which is ROM (Glue maps 8 bytes of ROM at FC0000-7 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM (FC0000-FEFFFF). The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse).
2. Read the longword at cartridge address FA0000. If the data read is a "magic number", execute from the cartridge (diagnostic cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations were previously written), initialize the memory controller, and continue running the application which was running before the reset if it was a warm start.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.
6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if succeeded.

SYSTEM ERRORS

The 68000 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen (mushroom clouds in older versions of disk loaded operating system). The number of bombs equals the number of the exception which occurred.

System errors may or may not be recoverable. Errors in loading files from disk will cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

NUMBER OF BOMBS AND MEANINGS
(No. 26,28,30, and 64-79 will not bomb, as they are legitimate.)

2 Bus Error. Glue asserted bus error or CPU detected an error.
3 Address Error. Processor attempted to access word or long word sized data on an odd address.
4 Illegal Instruction. Processor fetched an instruction from ROM or RAM which was not a legal instruction.
5 Zero Divide. Processor was asked to perform a division by zero.
6 Chk Instruction. This is a legal instruction, if software uses this, it must install a handler.
7 Trapv Instruction. See Chk instruction.
8 Privilege Violation. CPU was in user mode, tried to access a location in supervisor address space.
9 Trace. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.
10 Line 1010 Emulator. CPU read pattern 1010 as an instruction. Provided to allow user to emulate his own instructions.
11 Line 1111 Emulator. See Line 1010 Emulator.
12-23 Unassigned, should be no occurrence.
24 Spurious Interrupt. Bus error during interrupt processing.
25-31 Autovector Interrupt. Even numbered vectors are used, others should have no occurrence.
32-63 TRAP Instruction. The CPU read instruction which forced exception processing.
64-79 MFP interrupts.
80-255 User interrupts.

Note: If you have an error message such as "TOS ERROR 35", then the possible errors are:

1- The file in progress is bad.
2- The total number of folders in the system has exceeded the 40-folder limit. However, there is a program which can be used to extend this limitation on folders.
3- No handles left or too many open files.

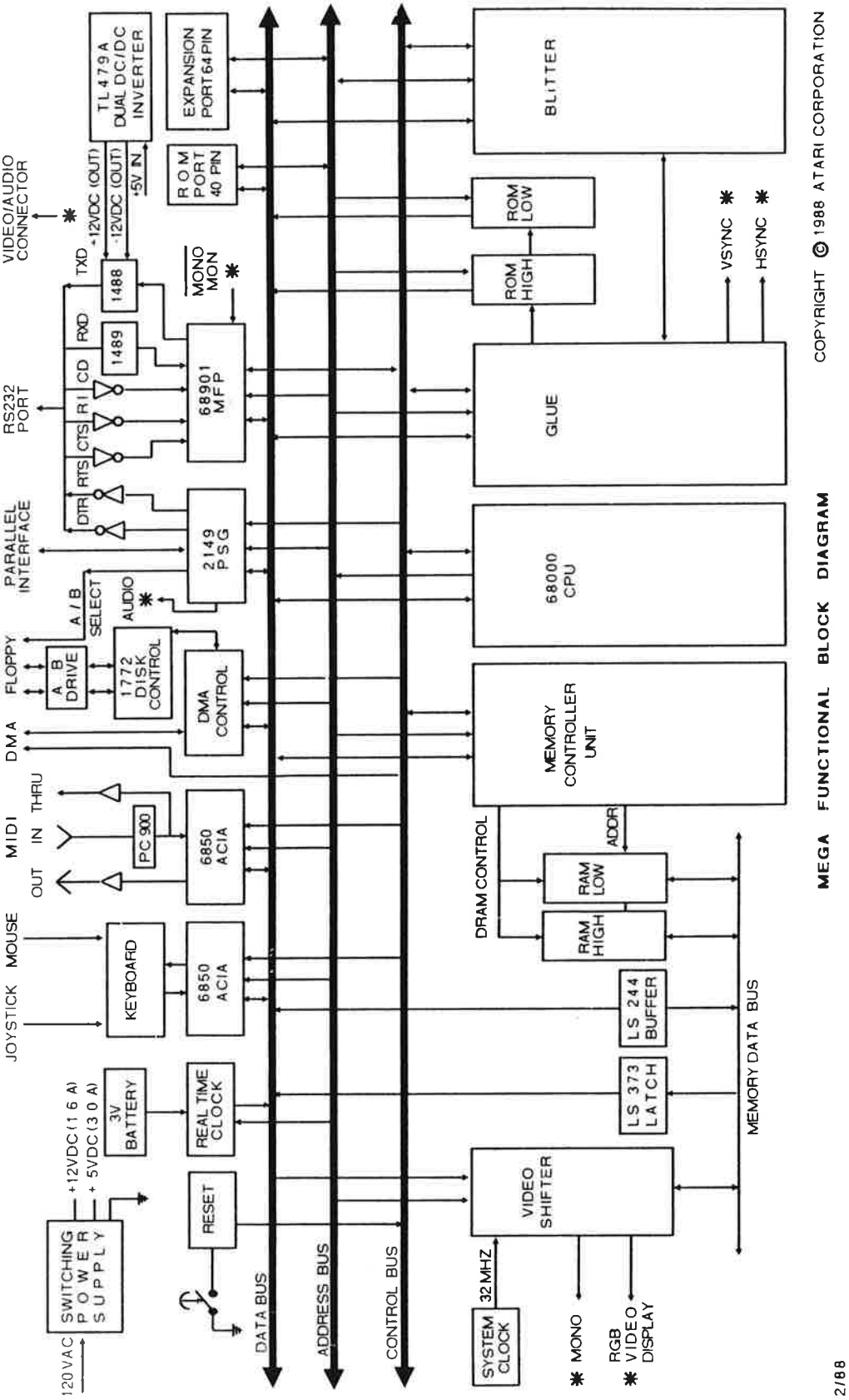


FIG. 15
FUNCTIONAL BLOCK DIAGRAM

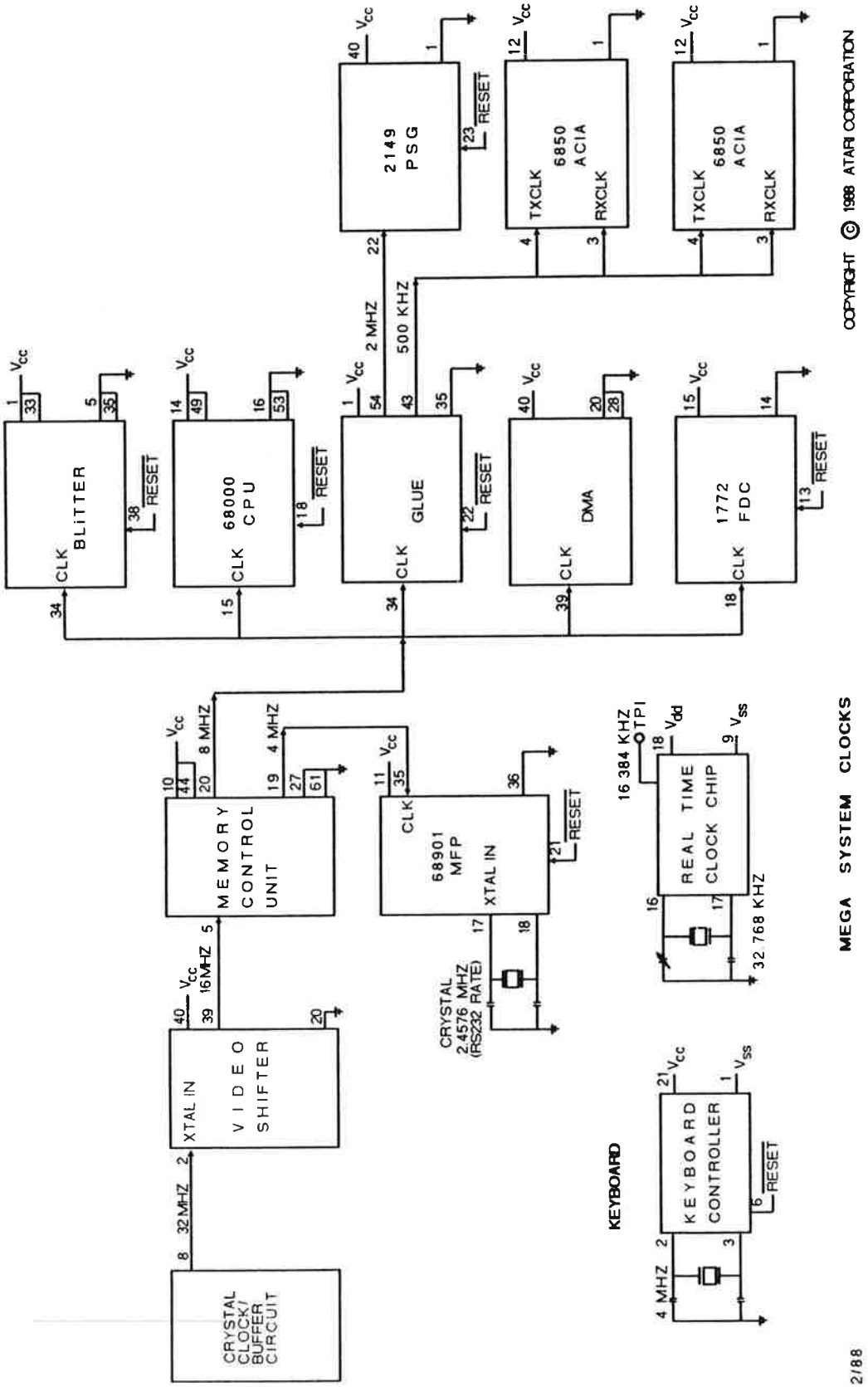


FIG. 16
SYSTEM CLOCKS

SECTION THREE
TESTING

OVERVIEW

This section pertains to the test equipment, diagnostic software, and test procedures used to verify correct operation and repair the Mega/ST computers. The diagnostic cartridge should be used if possible. If the unit gives no display or RS232 output when running the cartridge, see "Troubleshooting a Dead Unit" below.

Since the level of complexity in the Mega/ST system is high, it shouldn't be expected that this document can cover all possible problems or pinpoint the causes; rather, the intent here is to give a systematic approach which a technician can use to narrow down a problem to its most likely source. Experience in troubleshooting computer systems is assumed. Knowledge of the 68000 processor may be helpful. Economics will be an important consideration; due to the low cost of the Mega/ST computer line, little time can be justified in troubleshooting down to the component level when it may be cheaper to exchange the entire sub-assembly. Many of the more expensive (and critical) components maybe socketed, making verification and replacement faster.

TEST EQUIPMENT

The following equipment will be needed to test the Mega/ST computer:

* Atari SC1224 RGB Monitor (or similar)
* Atari SM124 Monochrome Monitor (or similar)
* Atari SF354 or SF314 Floppy Disk Drive
* Mega/ST Port Test Fixture
* Mega Expansion Test Fixture (Mega only)
* RS232 Loop-Back Connector
* MIDI Loop-Back Cable
* Mega/ST Test Diagnostic Cartridge (Revision 4.0)
* Diskettes (2)
* RS232 terminal (or Mega in VT52 emulator mode)

In addition, the following items will be necessary to troubleshoot and repair failed computers:

* Oscilloscope (100MHz Reccommended)
* Digital Multimeter, 1% FS (or better)
* Small Hand Tool, & Soldering Iron
* Spare Parts

TEST CONFIGURATION

With the power switch off, install the Diagnostic Cartridge (IMPORTANT--if the cartridge does not have the plastic enclosure, BE SURE THE CARTRIDGE IS INSTALLED WITH THE CHIPS FACING DOWN). Connect cables from test fixture into the hard disk port, parallel port, and joystick / mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the RS232 and MIDI loopback connectors into their ports. Plug the color monitor into the monitor output (a monochrome can be used instead).

Power on the unit. Some tests will be run automatically; in a few seconds the menu screen should appear. If the screen appears, skip down to " Mega/ST Diagnostic Cartridge ", below. If not, read next section "Troubleshooting a Dead Unit".

If the unit is being used as a terminal for a host computer, it should be disconnected from the host before using the diagnostic; otherwise, the host may think someone is logging on, and will send messages which will act like keystrokes input to the diagnostic.

TROUBLESHOOTING A DEAD UNIT

In the event that the system is correctly configured and powered and no display appears, this is the procedure to use for determining the problem. This assumes elementary steps have been taken, such as checking the LED in the forward left corner of the computer to verify the unit is powered and making sure the monitor is working.

1. Connect a dumb terminal to the RS232 port of the unit under test (U.U.T.). You can use an Mega/ST running the VT52 terminal emulator program--see the owner's manual for setting up VT52. The cable should connect pin 2 (serial out) of the U.U.T to pin 3 (serial in) of the terminal, and vice versa. Connect pin 7 (ground) to pin 7. The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity (this is the default condition for the VT52 emulator).

Insert the Diagnostic Cartridge into the U.U.T., and power on the unit. If the Diagnostic Cartridge messages appear on the display of the terminal, use the diagnostic to troubleshoot the computer. If not, the computer will have to be disassembled to troubleshoot. Refer to "Diagnostic Cartridge" below for information on using the cartridge.

If no activity is seen on the RS232 port or display, continue with (2) next page.

2. Disassemble the computer so that the printed circuit board is exposed (see Section 4, Disassembly). Power up the computer. Using an oscilloscope, verify the 8MHz clock to the 68000 CPU (pin 15). Replace oscillator if necessary. Then check pin 17 (HALT) of the 68000 CPU. It should be a TTL high. If so, go on to 3 below. If not, the CPU is halted. The reasons may be: (1) bad reset circuit, (2) double bus error, 3) bad CPU. Check (1) by observing signal on input of the two inverters on the HALT line. Check (2) by observing pin 22 of the CPU (BERR) as the unit is powered on. It should be high always. If there are logic low pulses, some component is malfunctioning and Glue is generating the error. Verify the clocks to Glue and Memory Controller and replace these components to verify them (if socketed). If still failing, the CPU is unable to read ROM or there is a component which is not responding to a read or write by the CPU, probably the MFP 68901 or DMA Controller. The MFP should respond to an MFPCS with DTACK. The DMA chip should respond to FCS by asserting RDY. There is no way to check (3) other than by elimination of the other two possibilities, although a hot CPU (too hot to touch for more than a second) strongly indicates a bad CPU.

3. If the CPU is not halted, it should be reading instructions from ROM (cartridge, if installed) and data and address lines will be toggling. (If not, replace CPU.) At this point, there is the possibility that both the video and RS232 subsystems are failing. Verify the output of the MFP chip (pin 8) while powering on the unit with the cartridge installed. If data is being sent, trace it through the 1488 driver. Note that + and - 12v. is required for RS232. If all looks good, there may be something wrong with the connection to the terminal.

Verify also the output of the Video Shifter. If using an RGB monitor, check the outputs to the summing resistors (if external) for R, G, and B. Note that if BLANK is not going high, no picture will be possible. If using monochrome, check output pin 30. Also check the input to the MFP, pin 29, MONOMON. Note that if the CPU does not read a low on this signal on power-up, it will cause RGB output on the Video Shifter.

If the Video Shifter is outputting a signal, but the picture is unreadable, there is probably a problem with screen RAM. The cartridge should be used to diagnose this problem, with the RS232 terminal as a display device.

MEGA/ST DIAGNOSTIC CARTRIDGE

The diagnostic cartridge is used to detect and isolate component failures in the computers (520/1040 and Mega). There are several revisions; this document refers to revision 4.0. Users of earlier versions should refer to the appropriate Troubleshooting Guide. This section gives a brief guide to use with a description of each test, error codes or pass/fail criteria, and recommendations on repair.

Power-up

The diagnostic program performs several tests on power-up. In particular, the message "Testing MFP, Glue timing, Video will appear, and the screen will appear scrambled for a few seconds before the menu is printed. The screen will turn red (dark background in monochrome) if an error occurs in the initial testing, with a message indicating the failure. The lowest 2 Kbytes of RAM is tested on power-up; if a location fails, the error will be printed to the RS232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there is no stack or system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen may turn red). Repair RAM.

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS232 port. The diagnostic program looks for keystrokes from the RS232 device.

If the display is unreadable, the RS232 terminal should be used. All messages are printed to the RS232 port as well as the screen.

Test Menu

The normal screen will be dark blue with white letters. The test title and revision number are displayed at the top, with the amount of RAM and keyboard controller revision below, and a test menu below that. To select tests, the user types the keys corresponding to those tests, and then the return key. Many iterations of the test or tests chosen can be run by typing in the number of cycles just before typing RETURN. Typing a zero will cause the test sequence to run continuously. To stop a cycle before completion, hit the escape key (there may be some delay in some tests before the test stops). As each cycle completes, the total numbers of cycles will be displayed on the screen.

MAIN MENU

Mega and ST Field Service Diagnostic Test Rev. 4.0
© 1987, Atari Corporation
4M RAM Keyboard revision 2 60 Hz OS Version 2 USA NTSC

R	RAM Test	O	O.S. ROMs	C	Color
K	Keyboard	M	MIDI	S	Serial Port
A	Audio	T	Timing	D	DMA Port
F	Floppy Disk	P	Printer/Joy Ports	H	High resolution

G Graphics chip (Blitter)
L Real-time clock
X Expansion connector

Q Run All Tests
Z Run Internal tests (R,O,C,K,A,T,L,G)

E Examine/Modify memory
B Set RS232 rate
V Toggle video output--50/60 Hz
? Help

Enter letter(s), and RETURN

The "G", "L", and "X" selections will be highlighted if these devices are found at start-up time. These should be present in Mega systems only. (The "X" selection requires the expansion test fixture be installed, which requires disassembly). If these selections are made when not highlighted, the test will check for their presence, and test if found.

The 'Q' selection sequences through all the tests except for High resolution monitor. The 'Z' selection sequences through RAM, ROM, Color, Keyboard, and Timing tests. Selection 'E' enables the operator to examine or modify RAM or hardware registers. The 'B' enables the operator to change the baud rate on the RS232 port. Pressing the up arrow increases it, pressing the down arrow decreases it.

Pressing '?' or the HELP key brings up a brief synopsis of the cartridge functions.

After a test or series of tests completes, the pass/fail status and error report, if any, will be displayed. Press the space bar to return to the menu.

If multiple tests are selected, the sequence can be halted before completion by pressing the ESC key. At the completion of the current test, the sequence will halt, with the options of either continuing or returning to the menu. In some cases there will be a considerable delay before the current test completes and the keystroke is detected. (Up to 3 minutes with 4 meg of RAM.)

Summary of Tests

RAM TEST

RAM is tested in three stages: low 2 kbytes, middle (up to 64k), and from 64k to top. The test patterns used are: all 1s, all 0s, a counting pattern (data=low word of the address), reverse counting pattern (data=complement of address low word). The counting pattern is copied from the top and bottom of a 32 Kbyte buffer into the current 32 Kbytes of video RAM, then shifts video RAM to a new area, verifies the pattern, and repeats the test, until the top of RAM is reached. Finally, addressing at 64k boundaries is checked by writing unique pattern in last 256 bytes of each 64k block.

If an error occurs, the error code is displayed, followed by the address, data written, data read, and the bits which did not agree. E.g.: " R2 45603E W:603E R:613C bad bits: 1,8".

In units having more than one bank (i.e., 1040ST, MEGA4) the address as well as the bit position must be used to find the correct chip. The following table gives a correspondence between the addresses and banks for various models:

	520	1040	Mega 2	Mega 4
0-7ffff	bank 0	bank 0	bank 0	bank 0
80000-fffff		bank 1	bank 0	bank 0
100000-1fffff			bank 0	bank 0
200000-3fffff				bank 1

(A bank is a 16 bit wide group of RAMs. A bank may consist of 256k bit chips--256k x 16 = 4 Mbit or 512k bytes--or 1Mbit chips--1Mbit x 16 = 16 Mbit or 2 Mbytes.)

RAM ERROR CODES

Except where noted, repair by replacing the RAM chip corresponding to the indicated bit(s).

R0--low memory failed while setting up to run test.

R1--failed walking 1s or 0s.

R2--failed address (counting pattern).

R3--failed 64k boundary test. Probable failure in Memory Controller.

R4--failed while displaying area tested (video RAM).

ROM TEST

This test reads the configuration bytes of the operating system to determine the version, language/country, and TV standard (PAL or NTSC). All bytes from operating system ROMs are then read and the checksums are calculated. These values are compared against known value with checksums for this version to determine if good or bad. Six checksums are displayed, although there may be only two ROMs in the machine (some machines have six 128K ROMs; some have two 1 meg ROM'S).

The test fails if the checksum calculated does not match the checksum expected for the configuration byte found (e.g. Version 2, French). Incorrect checksums are indicated by a message. If an error is displayed, replace the corresponding ROM. In a two ROM set, replace the low ROM if any of L0, L1, or L2 showed an error, or replace the high ROM if any of H0, H1, or H2 showed an error.

New revisions of TOS will cause this test to fail if not incorporated into the current version of the diagnostic. If you receive TOS revisions before receiving the diagnostic revision, it will be necessary to verify the checksums yourself.

COLOR TEST

This test verifies the Video Shifter. Seven color bands are displayed: red, green, blue, cyan, magenta, yellow, and white. Each band consists of 8 levels of intensity. All 16 color palettes are represented, each palette is a vertical strip across the screen (strips should not be discernable, but each color should be a straight line across the screen). Because of the tight timing involved, keystroke interrupts will cause the display to jitter.

The operator should see that there are no gaps or missing scan lines in the display. If lines are missing, check the three outputs on the Video Shifter for that color, and verify the values of the resistors on the output. Too low a brightness setting on the monitor will cause the monitor not to distinguish between fine levels, making it appear there are only four levels being output.

The Video Shifter has three outputs for red (R0, R1, R2), green (G0, G1, G2) and blue (B0, B1, B2). Each of these triples is summed together by a resistor network to give eight levels of intensity for each color, depending on which of the outputs are on. The values of the resistors give different weight to each output. The value of the resistor at R0 is twice that of R1, which is twice that of R2. This allows us to get 8 equal steps on the summed outputs. For example, R0 on , R1 and R2 off = 1/8, R0 off, R1 and R2 on = 7/8. This signal then passes through a transistor amplifier, and from there to the video monitor connector. NOTE : this resistor network is incorporated into the full custom chip in later versions of the video shifter (C101608). Video shifter which has part number C101608 or C070713 has pin 1 connected to to signal line BLANK. Shifter with part number C025914 will have pin 1 connected to a pull-down resistor R144,10K, and signal line BLANK will be connected to diodes D9, D10, D11.

Symtoms and fixes:

1. Missing primary color. Check the output of the transistor amplifier. Q6 is blue, Q7 is green, Q8 is red. Look for a staircase pattern (eight levels of intensity). If the signal is there, trace forward to the video connector, if not, trace backward to the Video Shifter, until the faulty component is found.

2. Primary colors present, secondaries missing or incorrect. Replace the Video Shifter.

3. Coarse change in intensity (not a smooth dark to light transition). Replace Video Shifter or look for a short on the output of one of the three color outputs for the appropriate color.

4. Specks or lines on the screen. This can be caused by bad RAM; if RAM has been tested and is good, replace the Video Shifter.

5. Wavering display, horizontal lines not occurring in the same place every time. The processor may be getting extra interrupts (if the processor is required to handle additional interrupts, it will not have timer to change all 16 color registers during a horizontal scan time). Examine the MFP interrupt request (pin 32). There should be an interrupt every 126 microseconds (2 display lines) from Display Enable (pin 20). If additional interrupts occur, locate the source: the inputs at pins 22-29 should all be high. If no external (to the MFP) source for the interrupts is found, replace the MFP.

   NOTE: if the keyboard is not connected, the input to the 6850 will be low, causing continual interrupts.

KEYBOARD TEST

Two types of test are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. If multiple tests have been selected, only the self-test is run. The operator presses keys and observes that the corresponding character on the screen changes (reverses background color). The key will also be displayed in the lower half of the screen. The mouse buttons and four directions are also shown on the screen. Connect the mouse and move in any direction and the arrow will flicker. Any key clicks while the mouse is moving indicates a short.

The self-test checks communication between the CPU and the keyboard microcomputer, and checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

KEYBOARD ERROR CODES

K0--Stuck key. A key closure was detected while the keyboard self test was executing.

K1--Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time. The keyboard needs to be replaced or the communication channel through the 6850 is not functional.

K2--Keyboard status error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status. Replace the keyboard.

MIDI TESTS

This test sends data out the MIDI port, (data loops back through the cable) and reads from the input and verifies the data is correct. This also tests the interrupt from the 6850 through the MFP chip. The LED in the loopback cable will blink as data is sent (not all cables have the LED).

MIDI ERROR CODES

M0--Data not received. Trace the signal from the output of the 6850, through the drivers, loopback cable, and receivers to the input of the 6850. Replace the defective component.

M1--Write/Read data mismatch. The data written was not the same as the data read. Replace 6850.

M2--Input frame error. Bad 6850 or bad driver or receiver causing noisy signal.

M3--Input parity error. Bad 6850 or bad driver or receiver causing noisy signal.

M4--Input data overrun. The 6850 received a byte before the previous byte was read. Probable bad 6850, also can be caused by the MFP not responding to the interrupt request.

RS232 TESTS

First the RS232 control lines are tested (which are tied together by the loopback connector), then the data loopback is tested. Data is checked transmissing?receiving using a polling method first, then using interrupts.

Data is transmitted at 300, 600, 1200...19200 bps. Data transmission is performed by the MFP and the 1488 and 1489 driver and receiver chips. Interrupts are a function of the MFP. Control lines are output by the PSG chip and input on the MFP. Note that this test does not thoroughly test the drive capability of the port, as the RS232 device may require voltage swings of 12 volts & there are no load resisters in the serial port diagnostic connector. If the test passes, but the unit fails in use, it is likely that the 1488 or 1489 chips are bad.

RS232 ERROR CODES

Data transmission error:

S0--Data not received. Check signal path: MFP pin 8 to J6 pin 2 via 1488 to J6 pin 3 to MFP pin 9 via 1489.

S1--Data mismatch. Data read was not what was sent. Check integrity of the signal. May be bad driver, receiver, or MFP.

S2--Input frame error. Incorrect time between start and stop bits. Probable MFP failure.

S3--Input parity error. Input data had incorrect parity. Probable MFP failure.

S4--Input data overrun. A byte was received before the CPU read the previous byte. MFP failure or, less likely, Glue failure.

S5--No IRQ. CPU did not detect an interrupt by the MFP. MFP or Glue failure.

S6--Transmit error. MFP transmitter failed.

S7--Transmit error interrupt. An error condition was created intentionally to cause an interrupt, and MFP didn't respond.

S8--Receive error interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.

S9--RI/DTR connection. Signal sent at DTR is not detected at RI.

SA--DCD/DTR connection. Signal sent at DTR is not detected at DCD.

SB--RTS/CTS connection. Signal sent at RTS is not detected at CTS.

AUDIO TEST

Outputs a low to high sweep on each of the three sound channels. One cycle of each channel is performed. If a channel is missing, replace the PSG chip. If no sound is heard, verify the output of the chip with an oscilloscope, and trace the signal to the monitor output connector. If no output from the PSG, verify the PSG is being selected by running the printer port or RS232 test (these tests both select the PSG).

TIMING TESTS

These tests are run at power-up as well as being selectable from the menu. The MFP timers, the Glue timing for VSYNC and HSYNC, and the Memory Controller video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as this test is run. There are two tests which check the bus timing for the 1772 and PSG chips. An error message is printed to the screen, then the test is run. If the test passes, the message is erased. If not, a Bus Error will occur and the message will remain. If a terminal is connected to the RS232 port, the message will not be erased, but "Pass" will be printed.

TIMING TEST ERROR CODES

T0--MFP timer error. One or more of the four timers in the MFP did not generate an interrupt on counting down .

T1--Vertical Sync. Glue is not generating vertical sync in the required time period.

T2--Horizontal Sync. Glue is not generating horizontal sync in the required time period.

T3--Display Enable. Glue is not generating DE output or the MFP is not generating an interrupt.

T4--Video Counter Error. The memory controller is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes. (MMU)

T5--PSG Bus Error. The PSG chip is defective.

T6--1772 Bus Error. The 1772 chip is defective.

DMA TESTS

Four sectors (2048 bytes) of data are written to the RAM on the port test fixture via high speed DMA, then read back and verified. This test is repeated many times for RAM addresses throughout the range of RAM.

DMA TEST ERROR CODES

D0--DMA timed out. No DMA occurred due to faulty DMA Controller, Glue, or Memory Controller, or the HDINT interrupt was not processed by the MFP. The failure can be isolated by seeing if the DMA Controller responds to HDRQ from the test fixture with ACK. Verify the MFP by seeing that the HDINT input causes an INTR output from the MFP.

D1--DMA counter error. the number of bytes transferred was incorrect. The Memory Controller or DMA Controller is bad.

D2--Data mismatch error. The data received from the DMA port was not the same as the data sent. Replace the DMA Controller. If the problem persists, check the data lines to the port for opens and shorts. A third possibility is that a defective 1772 is loading the bus.

D3--DMA not responding. DMA controller could not respond to a data resquest from the external controller. Replace the DMA chip.

FLOPPY DISK TESTS

The Floppy Main Menu

```
Floppy disk drive routine
(WARNING -- all choices except 2,6,7 write to the disk)
1) Quick Test
2) Read Alignment Disk
3) Disk Interchange Test
4) Disk Exerciser
5) Check copy protect tracks (80-82)
6) Test Speed
7) Install disk drives
```

In single test mode, a menu is displayed showing seven options:

1. Quick test. For each disk installed, formats, writes, and reads tracks 0, 1, and 79 of side 0. If double sided, formats and writes track 79 of side 1 and verifies that side 0 was not overwritten. If no disks are installed, checks to see what drives are online and if they are double or single sided. To assure that the drive are correctly tested, the operator should install (menu option 6) before calling the test. Once the test is run, the drives become installed, and will be displayed on the menu screen (below the RAM size).

2. Read track. Continuously reads a track, for checking alignment with an analog alignment diskette. The track to be read may be input by the operator. If "Return" is pressed without entering a number, the default is track 40.

3. Interchangeability test. Checks to see if diskettes from two disk drives each can be read by the other disk drive.

4. Disk exerciser. A more thorough disk test; tests all sectors on the disk for an indefinite period of time.

5. Copy Protect Tracks. Tests tracks 80-82, which are used by some software companies for copy protection). Not all failures are cause for replacement because some manufacturers disk drives will not write to these tracks.

6. Test speed. The rotational speed of the drive is tested and displayed on the screen as the period of rotation. The acceptable range is 196-204 milliseconds. The highest and lowest values measured are displayed. The test stops when any key is pressed.

7. Install disks. Specify how many and what type of disks to test.

If more than one test is selected from the main menu, the floppy menu will not appear, but the Quick Test will be selected automatically.

FLOPPY TEST ERROR CODES

No floppies connected--the controller cannot read index pulses. The cable may be improperly connected, or the drive has no power, or the drive is faulty.

F0--Drive not selected. Drive was installed, but failed attempting restore (seek to track 0). Check connection of cables, power to drive. Verify the light on the front of the drive goes on. Listen for the sound of the head seeking (the slide on the diskette should open). If all this occurs, TR0 (pin 23 on the 1772) should go low. If so, check for an interrupt on pin 28 of the 1772. If none, replace the 1772. Else trace the interrupt to the MFP, verify that the MFP responds be asserting INTR. If the drive is not being selected (no light), check the PSG chip. Pin 20 should go low when drive A is selected, and pin 19 should go low when drive B is selected. If not, replace the PSG.

F1,F2,F3 errors of previous versions have been deleted. The error message now says "Error Writing" (or reading or formatting), and displays a more specific error message, e.g., "F9 CRC error".

F4--Seek error. Verify that the STEP, MO, and DIRC outputs from the 1772 are sent to the drive. Probable failure in the 1772, but the drive is also suspect.

F5--Write protected. Check the write protect tab on the diskette. If OK, verify that the WP input (1772 pin 25) is going low during the test; if it is, then the 1772 is defective; if not, the problem is with the disk drive.

F6--Read compare error. Data read from the disk was not what was supposed to be written. Check in the following order: diskette, disk drive, 1772, and DMA Controller.

F7--DMA error. DMA Controller could not respond to a request for DMA. Replace the DMA Controller. If error persists, check FDRQ while running the test. It should normally be low and go high with each data byte transferred. If stuck high, push the reset button and verify that MR (1772 pin 13) goes low. If not, trace RESET to its source. If MR is OK, but FDRQ is still stuck, replace the 1772.

F8--DMA count error. Replace the Memory Controller, if that does not fix it, replace the DMA Controller.

F9--CRC error. The diskette or disk drive may be bad, else replace the 1772.

FA--Record not found. The 1772 could not read a sector header. May be a bad diskette, drive or 1772. If the test fails drive A but not drive B, the 1772 is not at fault (likewise fails B not A).

FB--Lost data. Data was transferred to the 1772 faster than the 1772 could transfer to the DMA Controller. If DMA Port test passes, the 1772 is probably bad. The DMA Controller could also be at fault.

FC--Side select error--single sided drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.

FD--Drive not ready. The format/write/read operation timed-out. Probably a bad disk drive. Verify by checking another drive. Could also be a faulty 1772.

Soft Error = does not cause a failure after 1 retry. (If doesn't fail a second time.)

Hard Error = failed second retry. Unit will halt if you reach any of the following: 20 read errors, 20 write errors or 5 format errors.

PRINTER AND JOYSTICK PORT TESTS

The port test fixture is used to test the parallel printer port and joystick ports. The parallel port test writes to a latch on the test fixture and reads back data. The joystick port test outputs data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU. The cables connecting the joystick ports to the test fixture must not be reversed, or the printer and joystick tests will fail.

PRINTER/JOYSTICK ERROR CODES

P0--Printer port error. Data read from the printer port was not what was written. Verify that the data lines on the PSG chip (pins 6-13) are toggling when the test is run. If not, run the RS232 test. If the RI-DTR and DCD-DTR errors occur, the chip is probably not being selected. Check if the chip selects are being activated and the 2MHz clock is present. If the PSG is selected and not outputting signals, replace it. If the data lines toggle, verify continuity. Also verify that J11 (Joystick 0) pin 3 is pulled up. Verify the test fixture is good by testing another computer. If it is OK, replace the PSG.

P1--Busy input error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected. If the P0 error also occurs, see handling for that. Otherwise, look for a signal arriving at MFP pin 22 from J5 pin 11. If no signal at J5, the test fixture may be bad. Verify with another computer.

J0--Joystick Port 0. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 12,10,9,8 respectively.

J1--Joystick Port 1. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 7,5,4,3 respectively.

J2--Joystick time-out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, keyboard-CPU communication line, or a faulty test fixture. If the power-up keyboard test passes, this eliminates any problem with keyboard-CPU communication.

J3--Left button input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, also check continuity from J10 pin 6 to J12 pin 11.

J4--Right button input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, also check continuity from J10 pin 6 to J12 pin 6.

HIGH RESOLUTION MONITOR

If this test is selected while a color monitor is connected, a message is displayed to connect the monochrome monitor. The CPU waits for an interrupt from the MONOMON input to the MFP, and when received (the operator connects the monochrome monitor), changes the display to high resolution. The display screen shows horizontal and vertical lines, each 2 pixels in width. The screen will reverse every two seconds. When the operator sees the display is correct, he unplugs the monochrome monitor and re-connects the RGB monitor and the display should return to normal.

GRAPHICS CHIP (BLiTTER)

This tests the ability of the BITBLiT to move blocks of memory around and perform logical operations on the data. No patterns appear on the screen. Many different error messages are possible (G0-G13), but the action for any error is the same: replace the chip. A faulty BLiTTER may cause a BUS ERROR.

REAL-TIME CLOCK

The test saves the current time and date, and writes a new time, waits one second, and verifies that hours, minutes, seconds, etc. have all rolled over. The is repeated for another date to verify all registers.

EXPANSION CONNECTOR

This test, for Mega models, requires the expansion test fixture (the top cover and shield must be removed to install the test fixture). It tests the expansion interface, in part by software, and the remainder by LEDs. The data and address busses and interrupt lines are tested in software. The control lines from the CPU are tested with the LEDs. Most of the LEDs will go off after the system is turned on and the menu appears on the screen. Three LEDs will remain lit: BR (bus request), BG (bus grant) and BGACK (bus grant acknowledge). These should go off after (1) the expansion connector test is run and (2) either the DMA test or floppy test are run. The LEDs simply indicate that the line is toggling. A lit LED means the line is not changing.

The software tests three groups of signals: data bus, address bus, and interrupts.

The first test writes and reads the RAM on the test fixture, setting one bit high at a time, to check for open or shorted data lines. If an error is found, the message "EX0 bad bit" is displayed.

The second test writes an incrementing pattern (0,1,2,...) across address bits 0-15, then across address bits 16-23 to the RAM on the test fixture to check for open or shorted address bits. If an error is found, the message "EX1 external RAM error, low byte" or "EX2 external RAM error, high byte" is printed, depending on whether the error occurred in the low or high address.

The third test uses circuitry on the external test fixture to create interrupt requests. There are three interrupts: INT3, INT5, and INT7. If the appropriate interrupt does not occur when expected, then a message is displayed: "EX3 INT3 error, "EX4 INT5 error", or "EX5 INT7 error".

ERROR CODES QUICK REFERENCE

This is a brief summary of all error code which may occur when running the diagnostic.

INITIALIZATION (Errors occurring before the title and menu appear)

I1 RAM data line is stuck.
I2 RAM disturbance. Location is altered by write to another location.
I3 RAM addressing. Wrong location is being addressed.
I4 MMU error. No DTACK after RAM access.
I5 RAM sizing error. Uppermost address fails.
I6 .

EXCEPTIONS (may occur at any time)

E1--E5 not used
E6 Autovector error. IPL0 is grounded or 68000 is bad.
E7 Spurious interrupt. Bus error during exception processing. Device interrupted, but did not provide interrupt vector.
E8 Internal Exception (generated by 68000).
E9 Bad Instruction Fetch.
EA Address error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceded by a bus error or bad instruction fetch.
EB Bus error. Generated internally by the 68000 or externally by Glue. Usually caused by device not responding. Displays the address of the device being accessed.

RAM

R0 Error in low memory (first 2K), possibly affecting program execution.
R1 Error in RAM chip.
R2 Address error. Bad RAM chip or memory controller. Address line not working.
R3 Address error at 64k boundary.
R4 Error during video RAM test. Bad RAM chip.

KEYBOARD

K0 Stuck key
K1 Keyboard controller is not responding.
K2 Keyboard controller reports error.

MIDI

M0 Data not received.
M1 Data received is not what was sent.
M2 Data input framing error.
M3 Parity error.
M4 Data overrun. Byte was not read from the 6850 before next byte arrived.

RS232

S0 Data not received.
S1 Data received is not what was sent.
S2 Data input framing error.
S3 Parity error.
S4 Data overrun. Byte was not read from the MFP before the next byte arrived.
S5 IRQ. The MFP is not generating interrupts for transmit or receive.
S6 Transmitter error--MFP.
S7 No interrupt from transmit error (MFP).
S8 No interrupt from receive error (MFP).
S9 DTR--RI. These signals are connected by the loopback connector. Changing DTR does not cause change in RI.
SA DTR--DCD. Same as S9 for these signals.
SB RTS--CTS. Same as S9 for these signals.

DMA

D0 Time-out. DMA did not take place, or interrupt not detected.
D1 DMA count error. Not all bytes arrived. Possible Memory Controller error.
D3 DMA Controller not responding.

TIMING

T0 MFP timers failed.
T1 Vertical sync timing failed.
T2 Horizontal sync timing failed.
T3 Display Enable Interrupt failed.
T4 Memory Controller video address counter failed. (Vain 68000).
T5 PSG Bus test. PSG chip is causing a bus error by staying on the data bus too long.
T6 1772 Bus test. 1772 chip is causing a bus error by staying on the data bus too long.

PRINTER AND JOYSTICK PORTS

P0 Printer port error.
P1 Busy (printer port input) failed.
J0 Joystick port 0 failed.
J1 Joystick port 1 failed.
J2 Joystick (keyboard controller) timed-out.
J3 Left button line failed.
J4 Right button line failed.

FLOPPY DISK DRIVE

F0 Drive offline. Not responding to restore (seek track 0).
F1 Format error.

(Note: former F2,F3 write and read errors are deleted. The message now will say "error writing" [or reading] and display the specific error found.)

F4 Seek error.
F5 Write protected.
F6 Data compare. (Data read not equal to data written.)
F7 DMA error.
F8 DMA count error (Memory Controller counter.)
F9 CRC error.
FA Record not found.
FB Lost data.
FC Side select error.
FD Drive not ready. Timed-out performing the command.

SECTION FOUR
DISASSEMBLY/ASSEMBLY

MEGA/ST DISASSEMBLY

Top Cover Removal:

1) Remove keyboard connector from the side of the top cover.

2) Turn unit upside down.

3) Remove the 9 screws from the square holes. These fasten the top case to the bottom. If the printed circuit board is to be exposed, or the disk drive is to be removed, also remove the three screws from the round holes. These hold the disk drive in place.

4) Turn the unit upright. While lifting the top cover up slightly from the back, unplug the battery connector from underneat its left rear corner. Now the cover can be removed easily.

Upper Shield Removal:

1) Straighten the six twist tabs. Note that there is one located under the disk drive.

2) Lift the shield up from the back gentlely so that it will be free from anythings in the rear.

3) Push the disk drive up while lifting up the front of top shield out of the bottom cover and pull forward.

Disk Drive Removal:

1) Lift the disk drive slightly and unplug the power harness connector and the ribbon cable.

Power Supply Removal:

1) Remove the 2 screws at front corners of power supply.

2) Unplug the wire harness connector in the right front corner of the power supply.

3) Lift the power supply up out of the main assembly.

Removal of main assembly from bottom case:

1) If power supply has not already been removed, then follow the power supply removal section to remove it.

2) Remove the six studs which secure the I/O shield to the bottom case.

3) Lift the assembly up from the front and pull forward.

Removal of Shield From Printed Circuit Board:

1) Straighten six twist tabs. It may be necessary to pull the twist tabs away from the board slightly.

2) Remove the I/O shield in the back.

   Note: Now that the major components are exposed, this is a convenient configuration for troubleshooting. The keyboard and disk drive may be re-connected and placed off to the side if those components are needed.

3) Lift the printed circuit assembly away from bottom shield.

Mega/ST RE-ASSEMBLY

1) Place insulation panel on bottom shield.

2) Attach the I/O shield to the I/O ports. Place Main Board on top of Bottom Shield over insulator panel.

3) Place the assembly in lower plastic case.

4) Secure the I/O shield to the bottom case with the 6 studs.

5) Plug in power supply connector and position power supply with tabs in slots.

6) Place assembly in lower plastic case.

7) Fasten the power supply to the bottom case at both front corners with two screws. This can be done with the power supply shield in place, using a magnestized screwdriver to hold the screw, or by removing the shield.

8) Plug disk drive power and ribbon cables into drive (cables go under shield), and position drive over standoffs.

9) Push the battery connector up from the opening located in the left rear corner of the top shield.

10) Align tabs on bottom shield with slots on top shield and fit top shield over main assembly. Twist the tabs to lock in place.

11) Place the top cover over the assembly.

12) Turn over the assembly and replace the 9 screws. The three longer screws go into the round holes to secure the disk drive.

A WORD OF CAUTION

It is strongly recommended that the computer be retested once in plastic to make sure that the re-assembly was done correctly and there are no shorts to Shield.

SECTION FIVE
SYMPTOM CHECKLIST

This section gives a brief summary of common problems and their most probable causes. For more detail, refer to the section on troubleshooting in this document, or the Diagnostic Cartridge Troubleshooting Guide.

Symptom	Probable Cause
DISPLAY PROBLEMS	
Black screen	No power (check LED), bad Glue chip, bad Video Shifter. See TESTING section, "Troubleshooting a Dead Unit".
White screen	Video Shifter, Glue, Memory Controller, DMA Controller, 68000. Use diagnostic cartridge with terminal connected via RS232 port.
Dots/bars on screen	RAM, Memory Controller, Video Shifter. Use diagnostic cartridge.
One color missing	video summer, buffer, Video Shifter. Check signals with oscilloscope.
Scrambled screen	Glue, Memory Controller. Use the diagnostic cartridge.
T.V. output bad	Modulator, phase locked loop. Trace the signal with your oscilloscope.
DISK DRIVE PROBLEMS	
Disk won't boot	Power supply, FDC (1772), DMA Controller, PSG chip, disk drive. See if select light goes on, if not, check PSG outputs. Listen for motor spinning. If not, check the power supply. Swap disk drive or try an external drive. If not working, check DMA Controller and 1772 with the diagnostic cart.
Disk won't format	FDC(1772), DMA Controller, disk drive.
System crash after loading files	Diskette, disk drive, FDC (1772), DMA, or Memory Controller. Swap diskette, retry. Use the diagnostics to check FDC (1772), DMA Controller, Memory Controller; or replace disk drive.

Systoms	Probable Cause
KEYBOARD PROBLEMS	
Keys won't work	Bad keyboard controller, 6850, MFP.
Keys won't work but mouse does	Keyboard cable was inserted while unit was powered, recycle power.
MIDI PROBLEMS	
No data	Bad opto-isolator chip, 6850, inverter (74LS04 , 74LS05).
RS232 PROBLEMS	
No data	Bad 68901 MFP, receiver, driver, or PSG chips, +/- 12v supply is blown. Use diagnostics to isolate bad line(s).
PRINTER PORT PROBLEMS	
No output	Bad PSG, MFP chips.
Does not output to a specific printer	Input impedance of printer is less than 3K ohm ,modify pullup resistors on printer.
DMA PORT PROBLEMS	
Does not function	Bad DMA Controller, Memory Controller, 1772 (loading the bus).
REAL TIME CLOCK PROBLEMS	
Does not function	Bad RTC PAL chip, clock chip, crystal.
Does not save time after cold boot	Bad batteries, power off sense circuit.
BLiTTER PROBLEMS	
No video when Blit is inserted	Jumpers below and to right of blitter chip must be cut before blitter will work.
Does not function	Replace blitter chip if above step doesn't fix problem.

SECTION SIX
DIAGNOSTIC FLOWCHARTS

This section summarizes in diagramatic form the steps taken in troubleshooting the Mega using the diagnostic cartridge. The details of using the cartridge are not shown; this shows the context in which the cartridge would be used, including some problems for which the cartridge would not be useful. Usage of the cartridge is covered in the troubleshooting guide. In general, the user would run all the tests, look up errors in the troubleshooting guide, and take the action recommended.

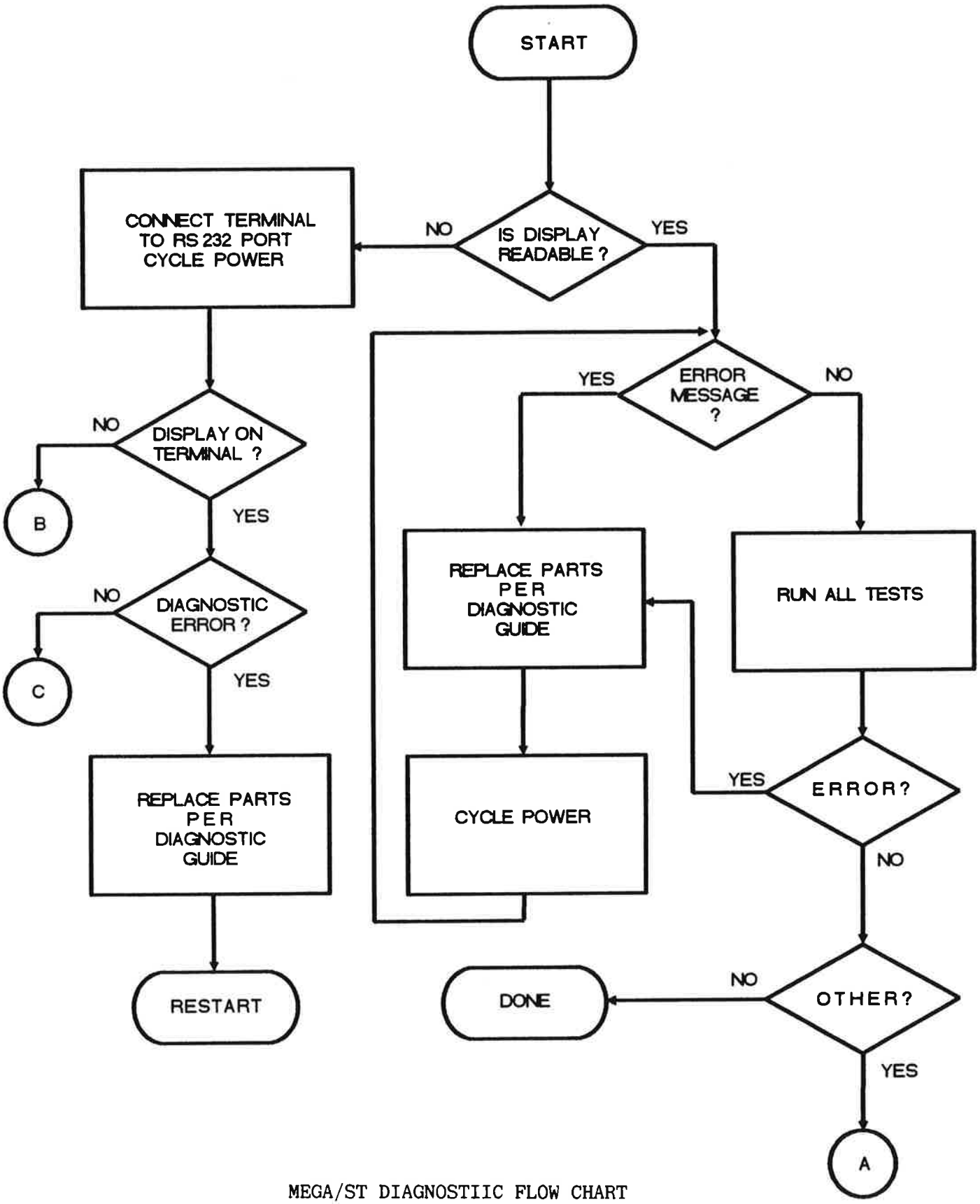
Although a thorough understanding of the system may be necessary in solving some problems, in most cases following the flowchart, reading the documentation on the diagnostic cartridge where necessary, and swapping out the indicated components will result in repair of the problem.

Replacement Procedures

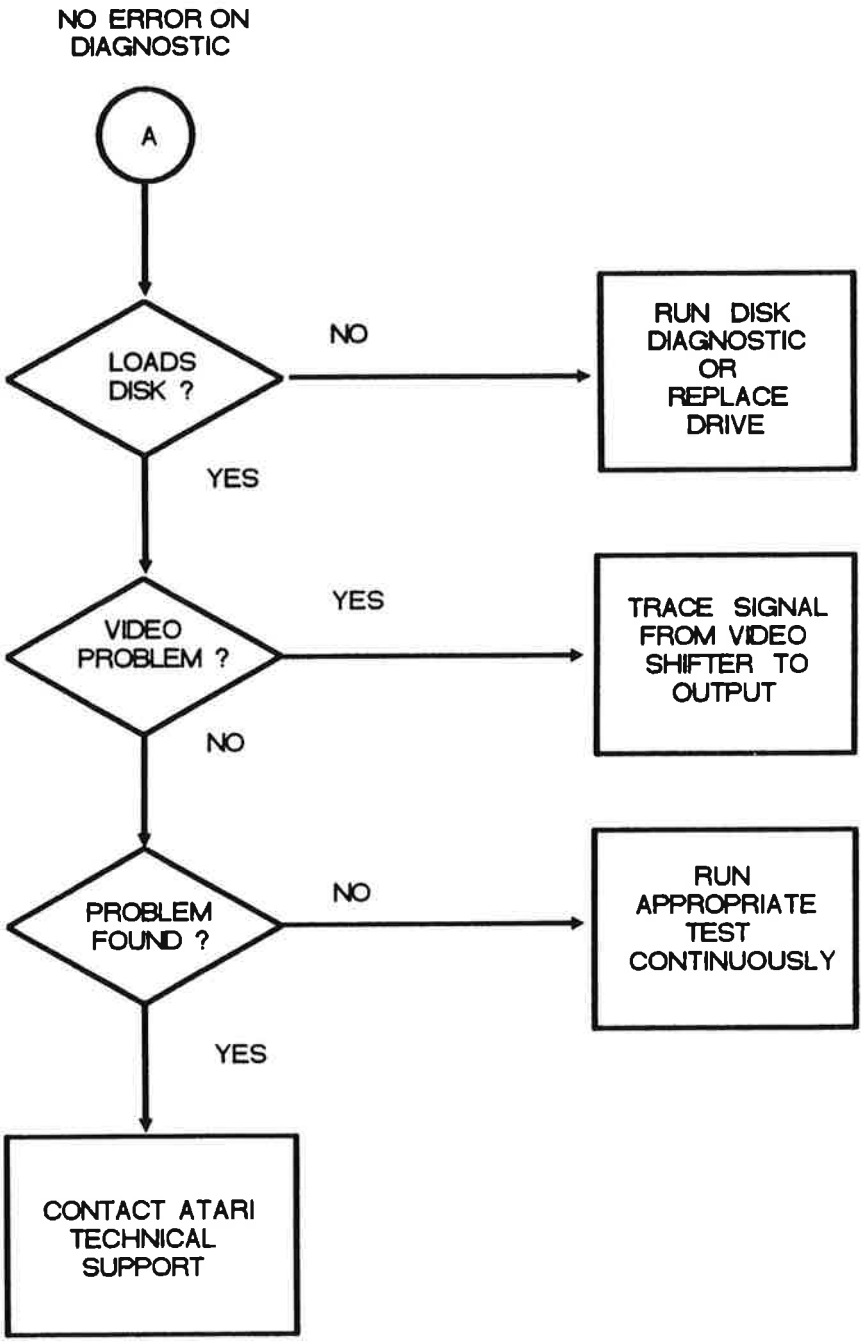
Where replacement is indicated, replace the component (if more than one is indicated, replace one at a time) with a known good part. If other components are later replaced, verify whether the first part is good by replacing in the system once the system has been repaired.

Handling of Integrated Circuits

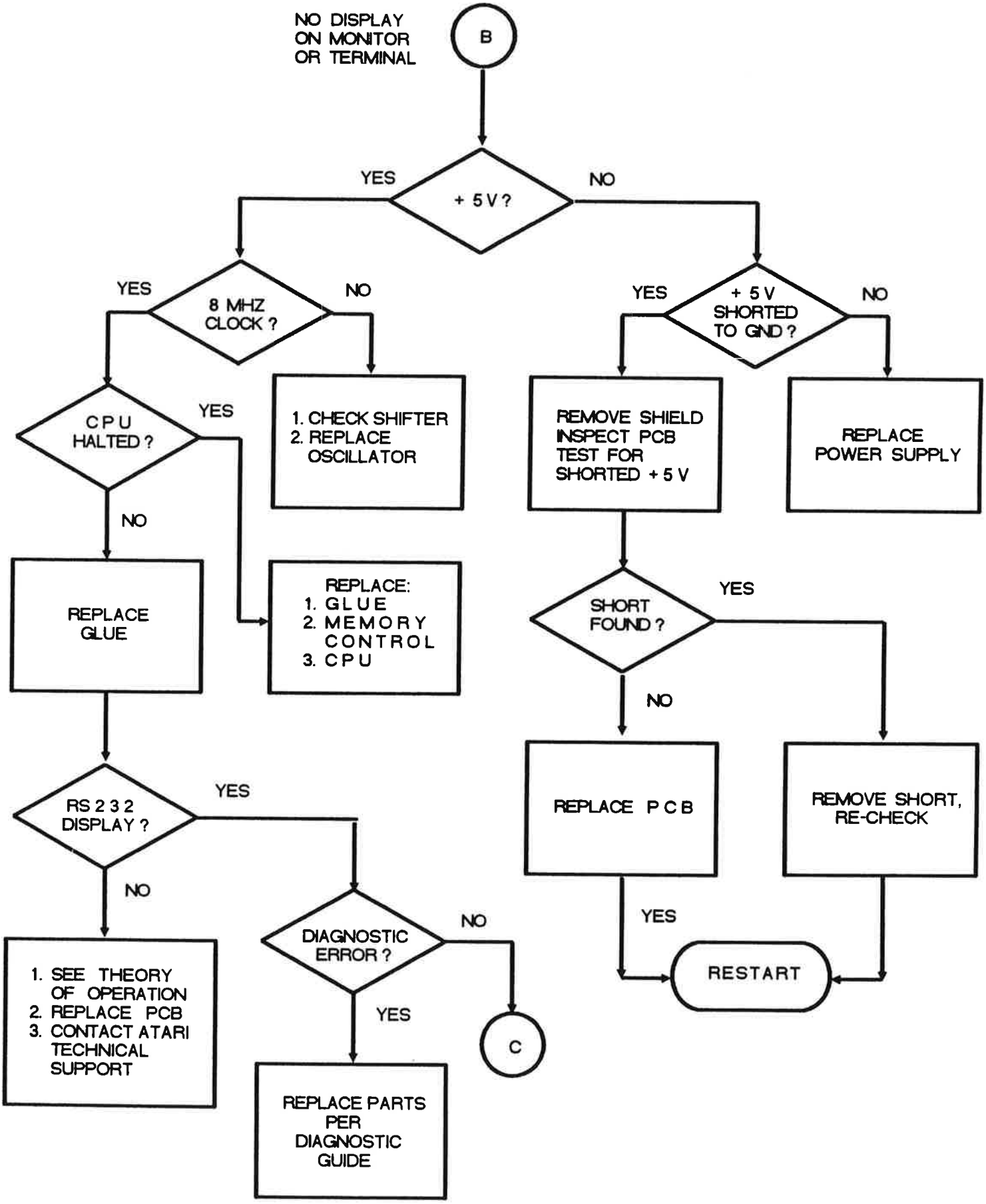
Extreme care should be taken when handling the integrated circuit chips. They are very sensitive to static electricity and can easily be damaged by careless handling. Keep chips in their plastic carriers or on conductive foam when not in use.

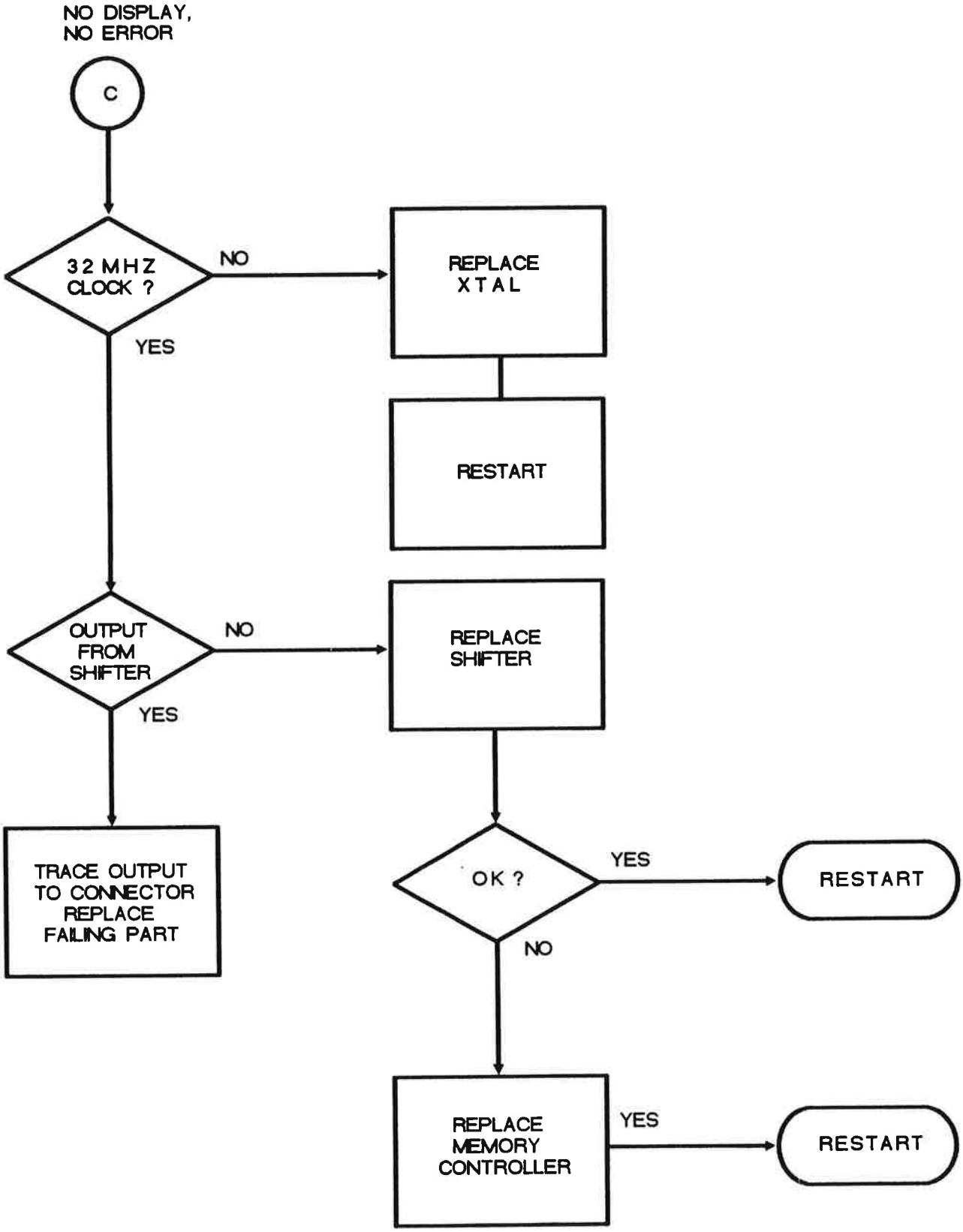


MEGA/ST DIAGNOSTIIC FLOW CHART



MEGA/ST DIAGNOSTIIC FLOW CHART


NO DISPLAY
ON MONITOR
OR TERMINAL
B
+ 5 V ?
YES
NO
8 MHZ
CLOCK ?
YES
NO
1. CHECK SHIFTER
2. REPLACE
OSCILLATOR
CPU
HALTED ?
YES
NO
REPLACE
GLUE
REPLACE:
1. GLUE
2. MEMORY
CONTROL
3. CPU
RS 232
DISPLAY ?
YES
NO
1. SEE THEORY
OF OPERATION
2. REPLACE PCB
3. CONTACT ATARI
TECHNICAL
SUPPORT
DIAGNOSTIC
ERROR ?
NO
YES
C
REPLACE PARTS
PER
DIAGNOSTIC
GUIDE
+ 5 V
SHORTED
TO GND ?
YES
NO
REMOVE SHIELD
INSPECT PCB
TEST FOR
SHORTED + 5 V
REPLACE
POWER SUPPLY
SHORT
FOUND ?
YES
NO
REPLACE PCB
REMOVE SHORT,
RE-CHECK
YES
RESTART



MEGA/ST DIAGNOSTIIC FLOW CHART

SECTION SEVEN
PARTS LISTS AND ASSEMBLY DRAWINGS

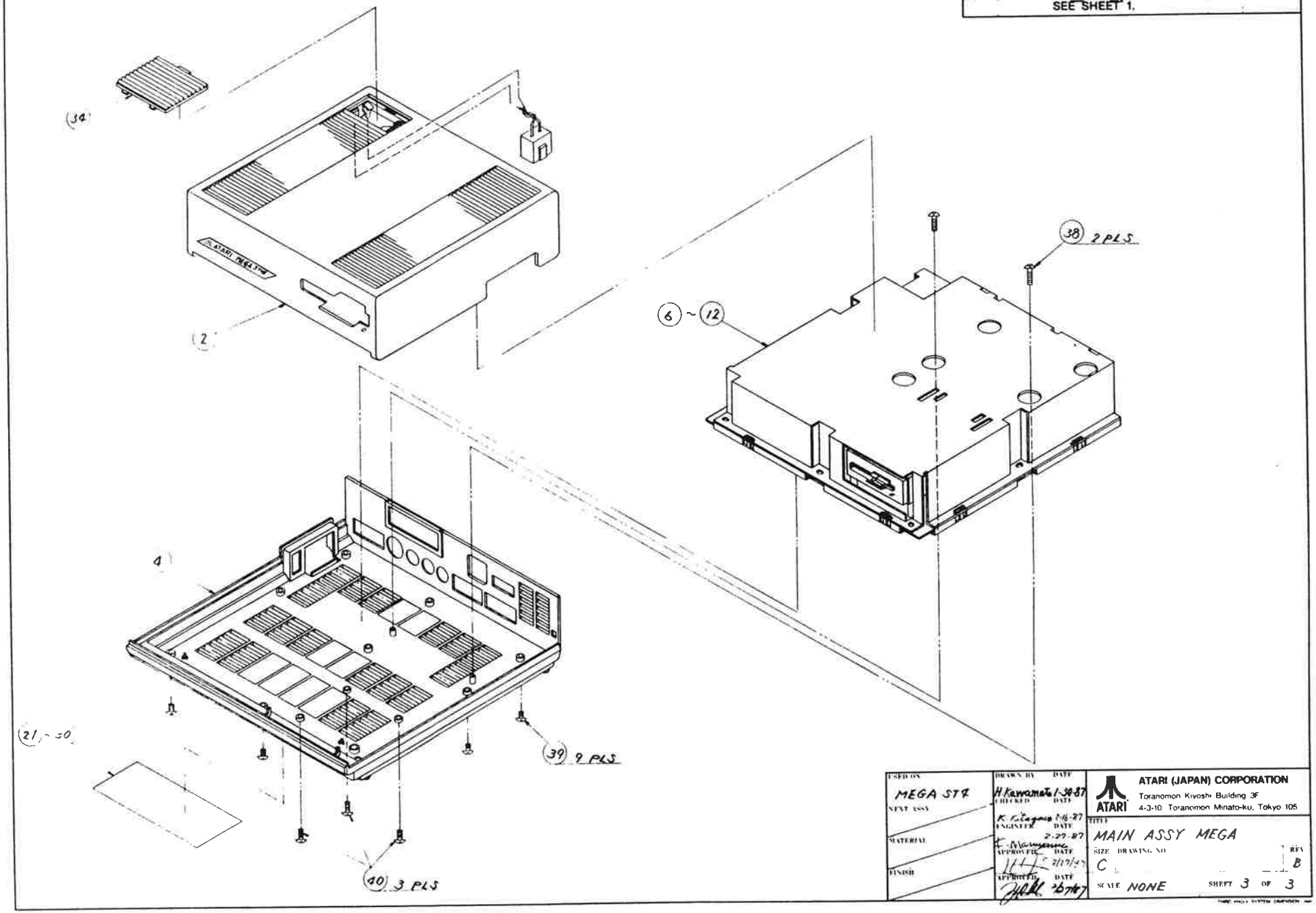
MEGA PARTS LIST

PART NUMBER	DESCRIPTION	LOCATION
CA200055-001	PCBA (1MB ROM) MEGA 4	SUBASSEMBLY
CA200093-001	PCBA (1MB ROM) MEGA 2	SUBASSEMBLY
CA200008-001	MEGA POWER SUPPLY w/FAN	SUBASSEMBLY
CA200018-001	MEGA 2/4 CASE BOTTOM	SUBASSEMBLY
CA200022-001	MEGA 2 CASE TOP	SUBASSEMBLY
CA200025-001	MEGA 4 CASE TOP	SUBASSEMBLY
CA200039-001	MEGA KEYBOARD COMPLETE	SUBASSEMBLY
CA200040-001	MEGA KEYBOARD CASE TOP	SUBASSEMBLY
CA200041-001	MEGA KEYBOARD CASE BOTTOM	SUBASSEMBLY
CA200042-001	MEGA KEYBOARD CONNECTOR PCBA	SUBASSEMBLY
CA200043-001	MEGA KEYBOARD (ONLY)	SUBASSEMBLY
CA200054-001	MEGA KEYBOARD CABLE	SUBASSEMBLY
C070350-003	FDD UNIT (1M BYTE) NEWTRONICS	SUBASSEMBLY
C070352-003	FDD UNIT (IM BYTE) CHINON	SUB FOR ABOVE
C103047-001	FDD UNIT (IM BYTE) CHINON	SUB FOR ABOVE
CA070025	STM1 MOUSE ASSEMBLY	ASSEMBLY
	CAP 30pF 50V ±5% CH. CER AXIAL	C39,40
	CAP 39pF 50V ±5% CH. CER AXIAL	C54
	CAP 100pF 50V ±5% SL. CER AXIAL	C43~46
	CAP 150pF 50V ±5% CH. CER AXIAL	C28
	CAP 330pF 50V ±10% B. CER AXIAL	C29
	CAP 1000pF 25V ±20% X. CER AXIAL	C68,69
	CAP 0.1µF 25VZ. CER AXIAL	C1,2,5~7,9~21,23,26 27,30~33,36,38,41, 42,47,48,50,52,55, 56,57,59,60,64~66, 70,73,112,113,120, 121~123
	CAP 0.22µF 50V Z5U. CER AXIAL	C80~95
	CAP 0.47µF 25V Z.CER AXIAL	C67
	CAP 4.7µF 25V ELEC AXIAL	C22,24,25
	CAP 10µF 16V ELEC AXIAL	C3
	CAP 47µF 16V ELEC RADIAL	C34,35
	CAP 100µF 16V ELEC AXIAL	C8,37,51
	CAP 1000µF 16V ELEC AXIAL	C140
	CAP 4700µF 16V ELEC RADIAL	C4
	CAP 1001µF 16V ELEC RADIAL	C49
	CAP 5-30pF TRIMMER	C53
	RES 0 OHM JUMPER	R120,123,126,145, 146,D12~14,W2,3
	RES 5.1 OHM 1/4W 5% CARBON	R15
	RES 27 OHM 1/4W 5% CARBON	R83
	RES 33 OHM 1/4W 5% CARBON	R52,54,55,57,60~66 68,76,110,113
	RES 47 OHM 1/4W 5% CARBON	R45~48
	RES 75 OHM 1/4W 5% CARBON	R67,73,77
	RES 100 OHM 1/4W 5% CARBON	R69,75,78,86,116
	RES 150 OHM 1/4W 5% CARBON	R23,115
	RES 220 OHM 1/4W 5% CARBON	R10,14,16,17,19,44
	RES 470 OHM 1/4W 5% CARBON	R26
	RES 1K OHM 1/4W 5% CARBON	R1,2,4,21,24,30,37 38,40~43,82,85,111
	RES 1.2K OHM 1/4W 5% CARBON	R20,76

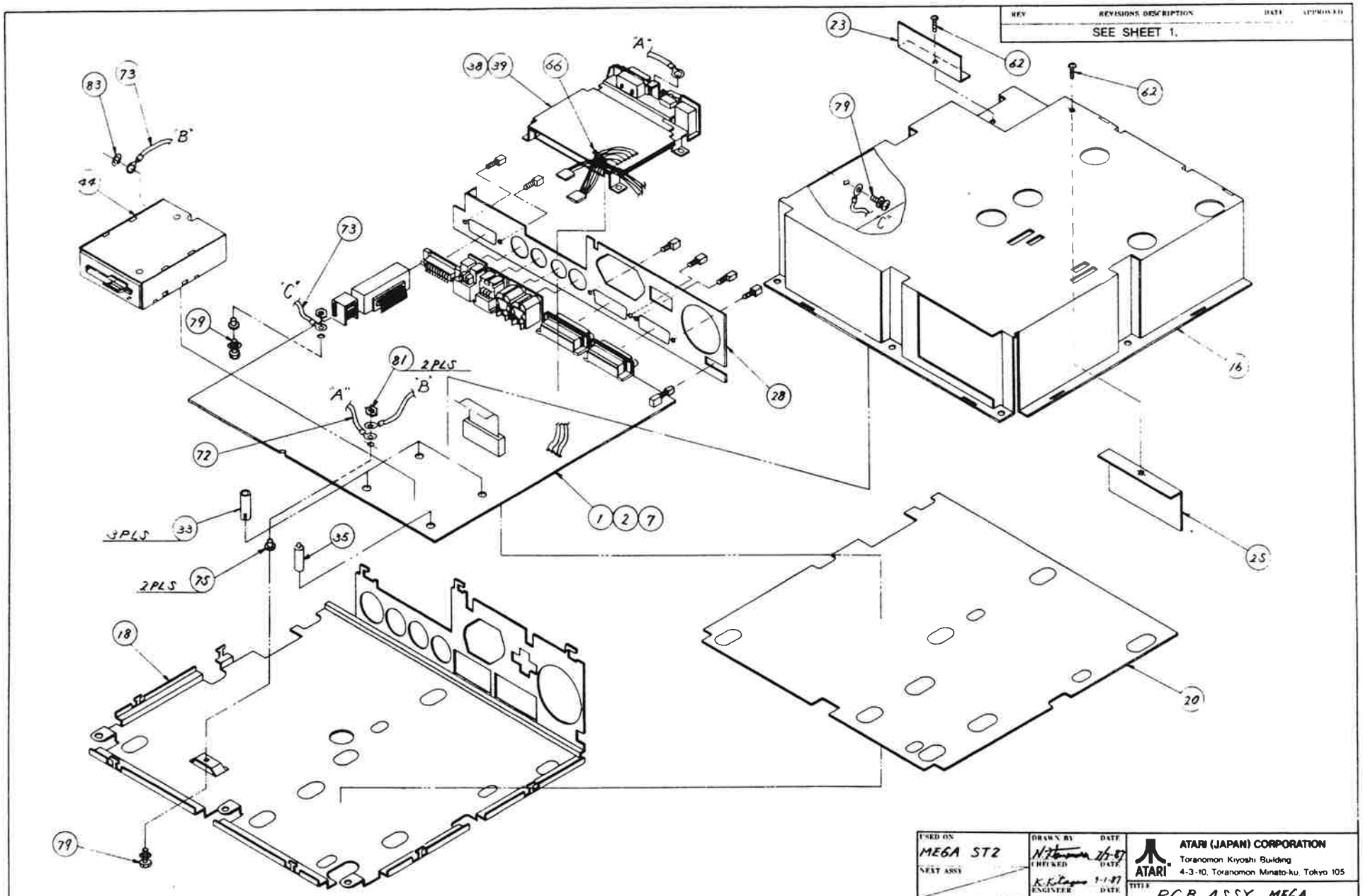
PART NUMBER	DESCRIPTION	LOCATION
	RES 2.2K OHM 1/4W 5% CARBON	R5
	RES 3.3K OHM 1/4W 5% CARBON	R27
	RES 4.7K OHM 1/4W 5% CARBON	R6,11,28,29,39,112
	RES 5.1K OHM 1/4W 5% CARBON	R22
	RES 10K OHM 1/4W 5% CARBON	R7,8,25,33~36,108, 109,114
	RES 12K OHM 1/4W 5% CARBON	R18
	RES 51K OHM 1/4W 5% CARBON	R32
C070567-004	RES NETWORK 1K OHM X 6	Rp7
C070159-006	RES NETWORK 4.7K OHM X 8	RP1~4
C070448	RES NETWORK 10K OHM X 8	RP5,6
C014384	INDUCTOR FERITE BEAD AXIAL	L1,12,45,46,48
C070205	INDUCTOR 0.27uH 20% AXIAL	L47
C070471-001	INDUCTOR 10µH 10% AXIAL	L50
C070471-002	INDUCTOR 220µH 10% AXIAL	L5
C070790	LINE FILTER	L9
C070241-002	NOISE FILTER ZJS5101-02	L2~4,6~8,13~22,24 ~30,32~43
	TRANSISTOR 2N3904	Q1,3,6~10
	TRANSISTOR 2N3906	Q2
	DIODE 1N914	D1~3,5~8,15~18
C101805	DIODE 1SS108 SCHOTTKY BARRIER	D4
C025993	CRYSTAL 2.4576 MHZ	Y1
C100232	CRYSTAL 32.768KHZ	Y2
C100281	CRYSTAL 32.0424 MHZ	OSC1
C070129	CONN 40 PIN RIGHT ANGLE	J2
C070130	CONN DB-19S HARD DISK	J10
C070131	CONN 14 PIN DIN FLOPPY DISK	J13
	CONN DB-25P RS232C	J7
	CONN DB-25S PARALELL	J6
C070134	CONN 13 PIN DIN VIDEO	J14
C070033	CONN 5 PIN DIN MIDI	J3,4
C070445	CONN SINGLE INLINE 6 PIN	J1,18
C070644-011	CONN DOUBLE INLINE 24 PIN	J17
C100283-001	CONN DOUBLE INLINE MALE 64 PIN	J15
	SOCKET 40 PIN	U27,31
	SOCKET 28 PIN	U3,4,6,7,9,10
C070120	SOCKET 68 PIN LCC	U5,17,30
C070119	PUSH SWITCH	S1
CA070024	FLAT CABLE 34P ASSEMBLED	J12
CA070023-003	CABLE 4P ASSEMBLED	J11
CA200053-002	CABLE ASSY:MALE TYPE 2 PIN	J9
C101643	IC CUSTOM ST BLITTER	U5
C025982	IC 68000-8 CPU	U8
C025913	IC CUSTOM DMA CONTROLLER	U27
C025915	IC CUSTOM GLUE	U17
C025914	IC CUSTOM SHIFTER	U31 or
C101608	IC CUSTOM FULL SHIFTER (w/D/A)	U31
C025912	IC CUSTOM MMU	U30
C025986	IC 1489 RS-232C, RECEIVER	U19
C025987	IC 1488 RS-232C, DRIVER	U20
C025983	IC YM2149, SOUND	U16
C025984	IC 68901, MFP	U18
C025985	IC 6850, ACIA	U14,15
C101712	IC DYNAMIC RAM 1M X 1	U40~55(60~75)
C025988	IC PC900 PHOTO COUPLER	U13

PART NUMBER	DESCRIPTION	LOCATION
C101621	IC TL 7705A	U1
	IC 74LS02, QUAD NOR	U21
	IC 74LS06, HEX INVERTER O.C.	U26
	IC 74LS07, HEX O.C. BUFFER	U2
	IC 74LS32, QUAD 2-INPUT OR GATE	U78
	IC 74LS148 8-3 PRIOR ENCODER	U39
	IC 74HC00 QUAD NAND GATE	U24
C101622	IC RP5C15 REAL TIME CLOCK	U25
C101625	IC RTCPAL PAL16L8	U37
	IC 74LS244.3 STATE LINE BUFFER	U32,35,58,59
	IC 74LS373 LATCH	U33,36
	IC 74LS11 TRIPLE 3-INPUT AND GATE	U12
C070447	IC TL497A SWITCHING REGULATOR	U22
C026028	IC WD-1772 FDD CONTROLLER	U28
C101629-001	IC; TOS ROM 1 MEG HI-0	U9
C101630-001	IC; TOS ROM 1 MEG LO-0	U10
C070349-002	AC POWER CORD (UL/CSA)	
C100296-001	MEGA MANUAL OWNERS	
C070322	COLLAR A	3 DRIVE SPACERS
C070323	COLLAR B	1 DRIVE SPACER

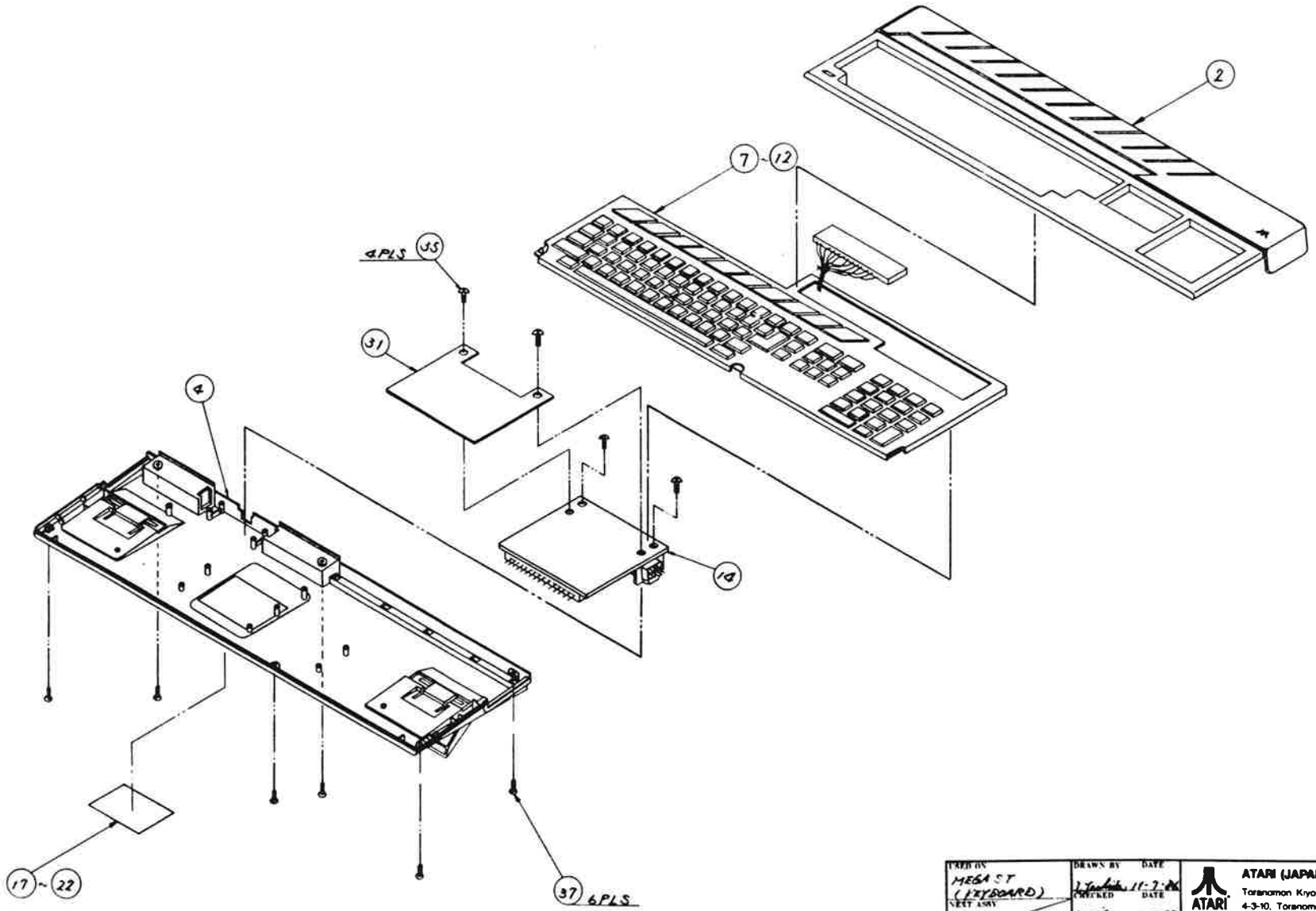
REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON: MEGA ST2	DRAWN BY: H.Kawamata 1-30-87	ATARI (JAPAN) CORPORATION
NEXT ASSY:	CHECKED: K.Kitagawa 1-6-87	Toranomon Kiyoshi Building 3F
MATERIAL:	ENGINEER: 2-27-87	4-3-10 Toranomon Minato-ku, Tokyo 105
FINISH:	APPROVED: 2/17/87	TITLE: MAIN ASSY MEGA
	APPROVED: 2/26/87	SIZE: C DRAWING NO: REV B
		SCALE: NONE SHEET 3 OF 3

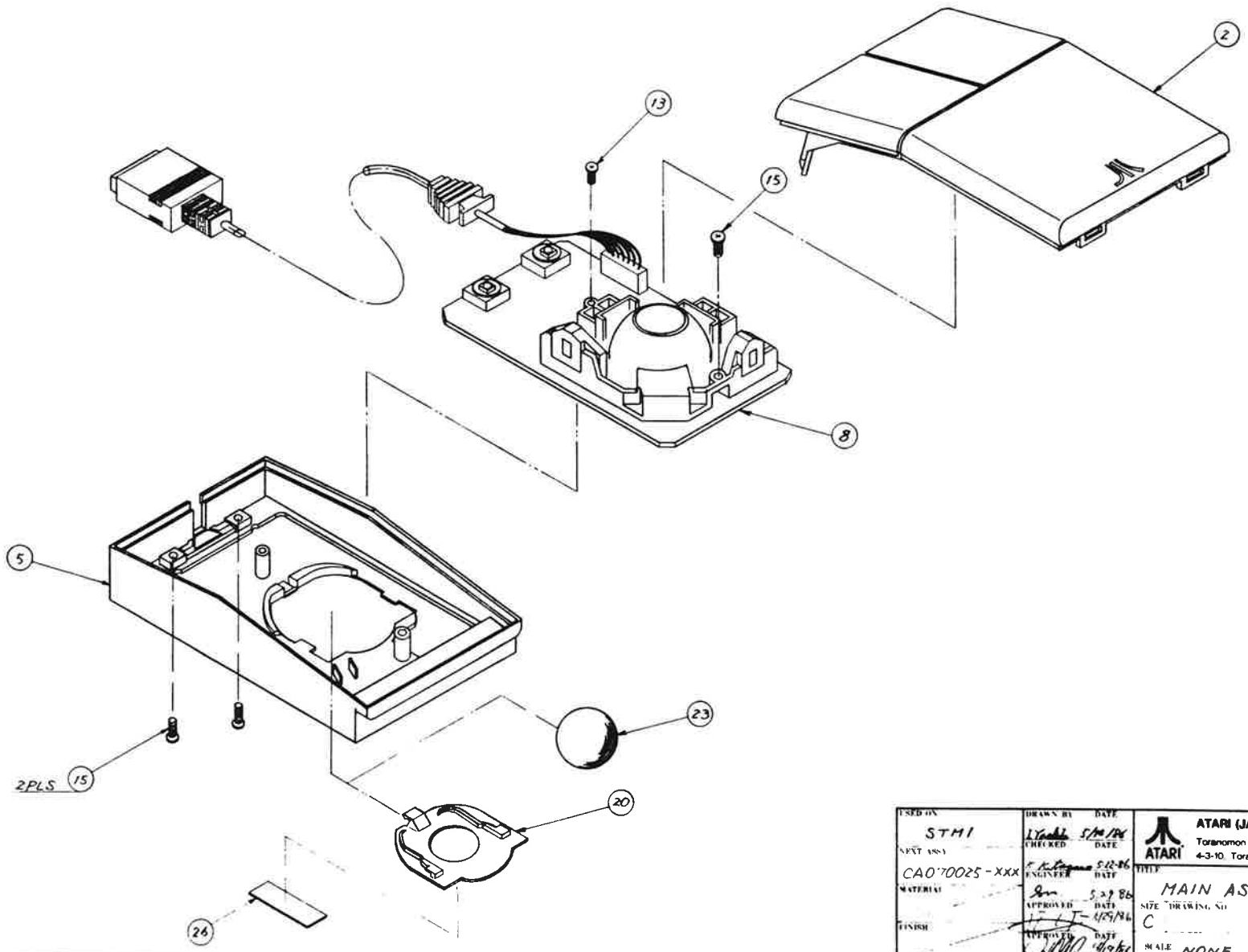

REV
REVISIONS DESCRIPTION
DATE
APPROVED
SEE SHEET 1.
2PLS
3PLS
2PLS
USED ON
MEGA ST2
NEXT ASSY
MATERIAL
FINISH
DRAWN BY
DATE
CHECKED
DATE
ENGINEER
DATE
APPROVED
DATE
APPROVED
DATE
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4-3-10, Toranomon Minato-ku, Tokyo 105
TITLE
PCB ASSY MEGA
SIZE
DRAWING NO
REV
C
A
SCALE NONE
SHEET 6 OF 6

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON: MEGA ST (KEYBOARD) SHEET ASSY	DRAWN BY: J. Tanaka 11-7-87 DATE	ATARI (JAPAN) CORPORATION Toranomon Kyoshi Building 3F 4-3-10, Toranomon Minato-ku, Tokyo 105
MATERIAL	CHECKED DATE	TITLE: KEYBOARD MAIN ASSY
FINISH	ENGINEER: T. Tsuyuguchi 11-10-87 DATE	SIZE: C DRAWING NO: MEGA REV: A
	APPROVED: H. Tsuji 11/21/87 DATE	SCALE: NONE SHEET 3 OF 3
	APPROVED: 12/6/87 DATE	

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON: STM1	DRAWN BY: I.Yoshi DATE: 5/14/86	ATARI (JAPAN) CORPORATION
NEXT ASSY: CA0'0025-XXX	CHECKED: K.Kitagawa DATE: 5-12-86	Toranomon Kiyoshi Building 3F
MATERIAL:	ENGINEER: DATE:	4-3-10, Toranomon Minato-ku, Tokyo 105
FINISH:	APPROVED: DATE: 5.29.86	TITLE: MAIN ASSY STM1
	APPROVED: DATE: 4/29/86	SIZE: C DRAWING NO: REV: B
	APPROVED: DATE: 6/9/86	SCALE: NONE SHEET 3 OF 3

SECTION EIGHT
SCHEMATICS AND SILKSCREEN

REV	REVISIONS DESCRIPTION	DATE	APPROVED
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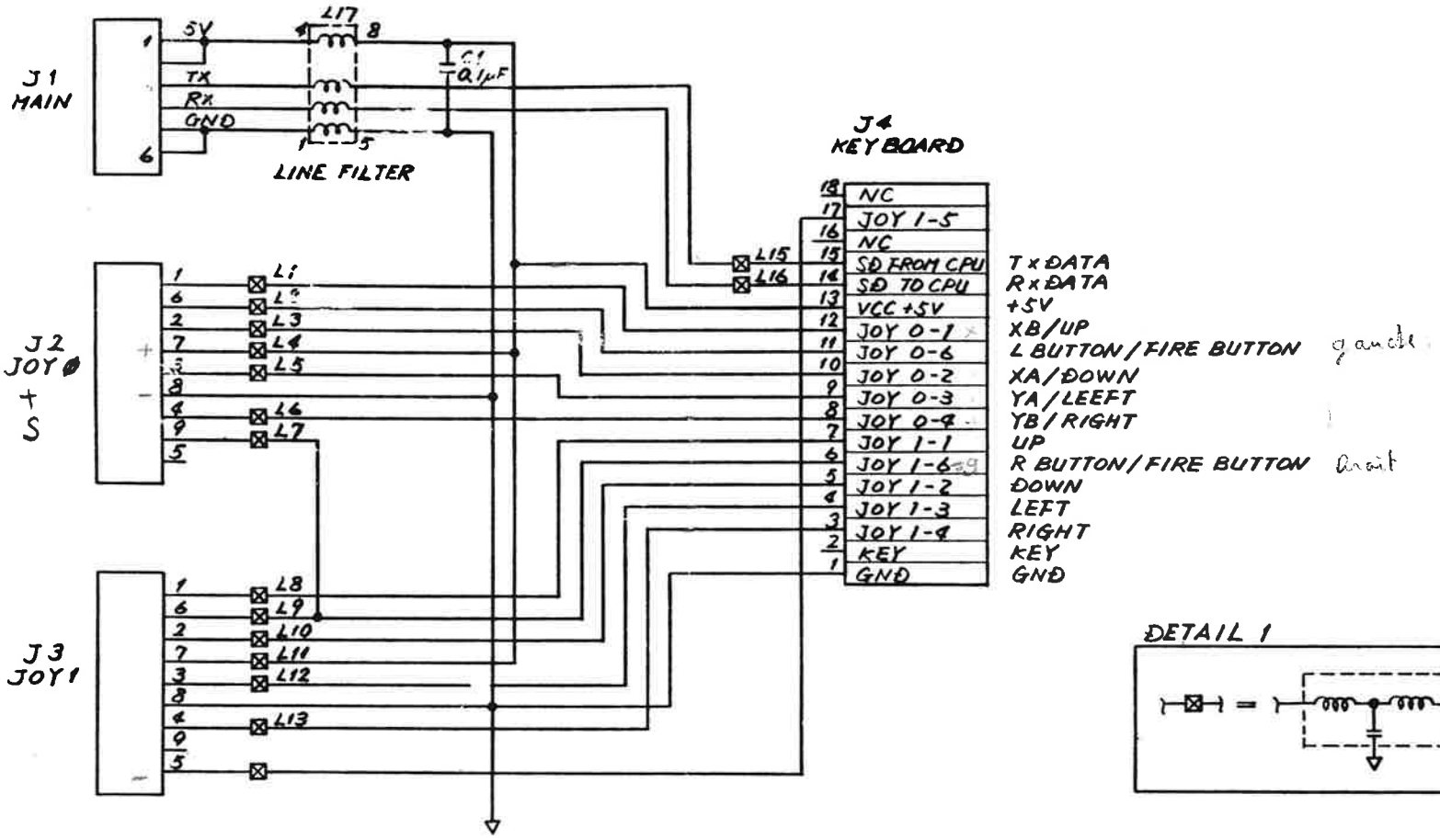


DETAIL 1

1. NOISE FILTER : SEE DETAIL 1 .

NOTES—UNLESS OTHERWISE SPECIFIED:

NEXT ASSY	USED ON
CA200092-XXX	MEGA ST (KEYBOARD)

APPLICATION

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4
MATERIAL	
FINISH	

	NAME	DATE
DRAWN BY	I. Yoshida	10-26-86
CHECKED	K. Kitagawa	10-27-86
ENGINEER	A. Shinogawa	2-16-87
APPROVED	S. OKAZAKI	2/18/87
APPROVED		2/17/87

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

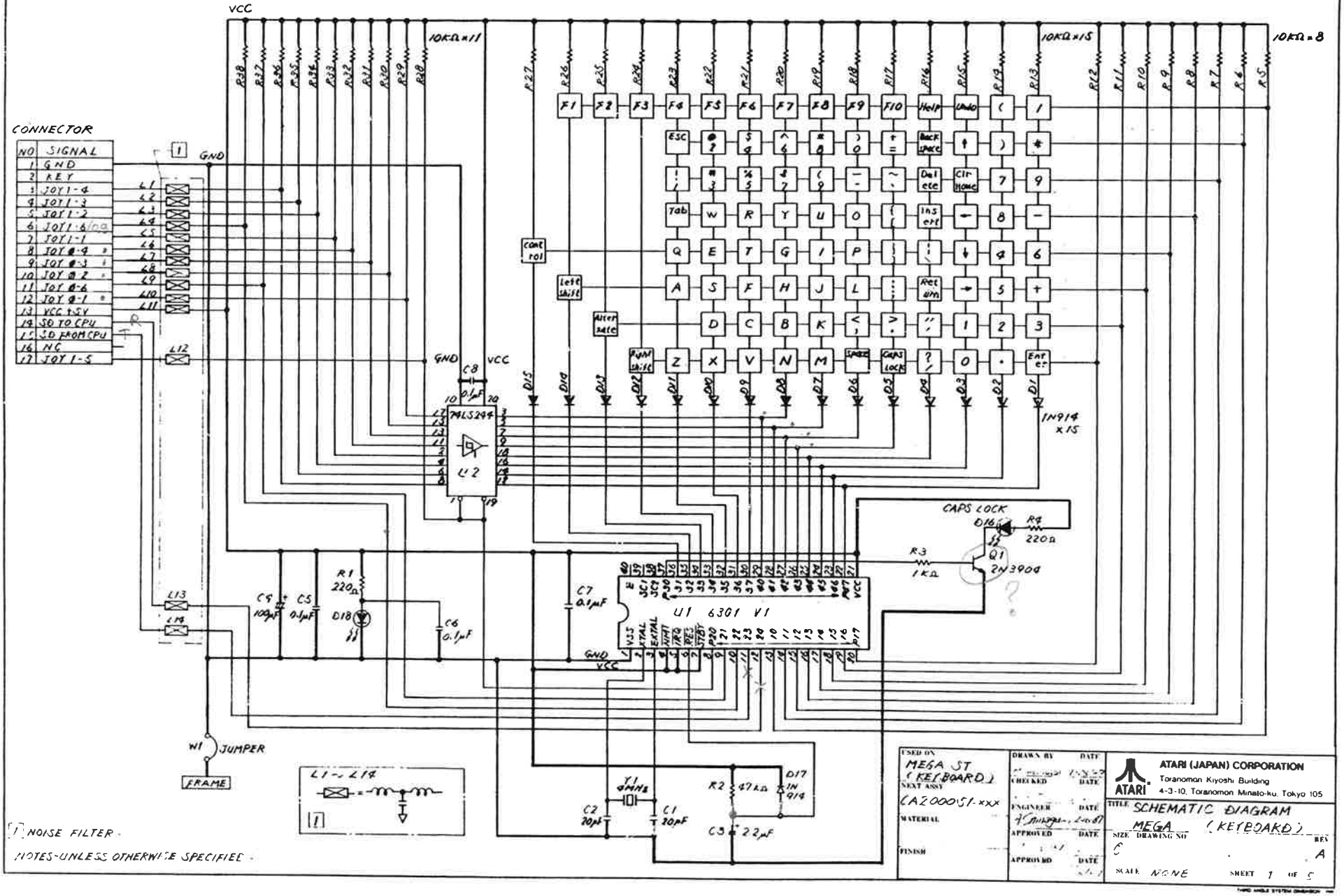
TITLE: SCHEMATIC DIAGRAM SUB PCB MEGA (KEYBOARD)

SIZE	DRAWING NO.	REV
B		A

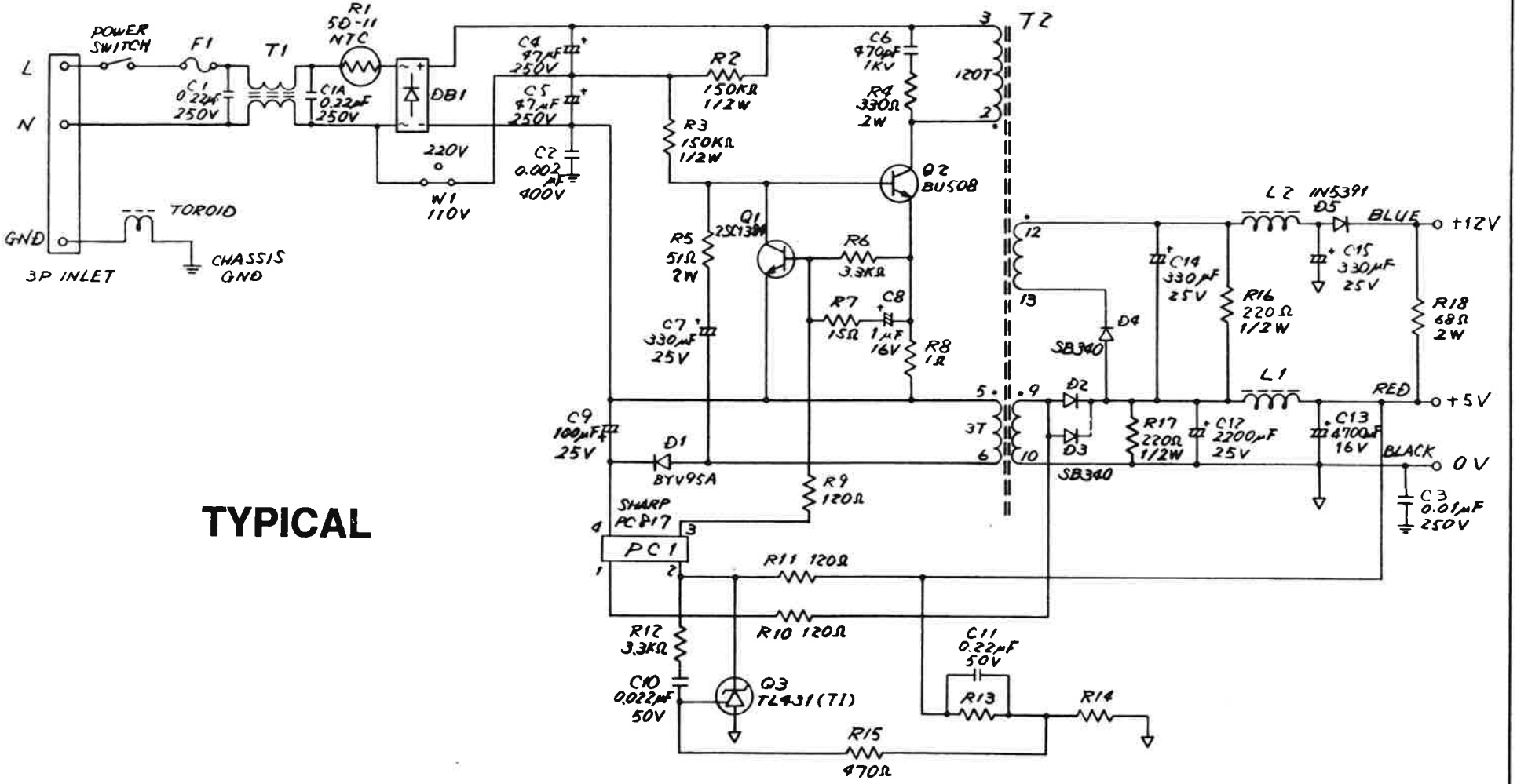
SCALE NONE | SHEET 1 OF 1

THIRD ANGLE SYSTEM. DIMENSION : mm

REV	REVISION DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	19.1	



REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	2/2/87	



TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

USED ON: ASP34-1
NEXT ASSY
MATERIAL
FINISH

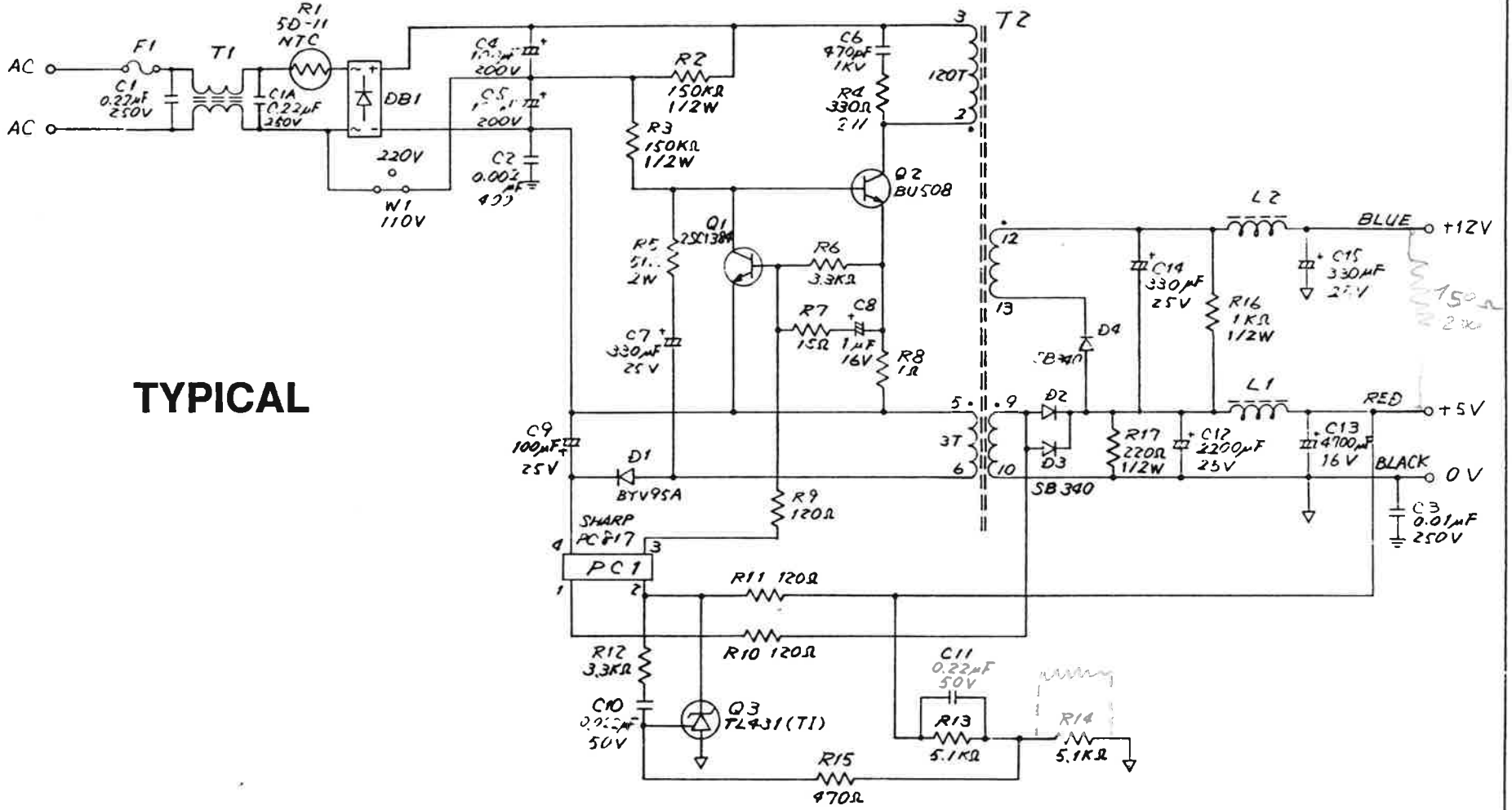
DRAWN BY I Yoshida DATE 9/23/86
CHECKED
ENGINEER K Kitagawa 9-18-86 A. Shimagawa 10-23-86 DATE
APPROVED DATE
APPROVED DATE 10/31/86

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

TITLE: SCHEMATIC DIAGRAM (ASP34-1)
SIZE B DRAWING NO. COMPUTER REV A
SCALE NONE SHEET 1 OF 1

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE		



TYPICAL

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

USED ON: ASP-3

NEXT ASSY

MATERIAL

FINISH

DRAWN BY	I. Yoshida	DATE 9/23/86
CHECKED		DATE 9/23/86
ENGINEER		DATE 10/23/86
APPROVED		DATE
APPROVED		DATE

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku Tokyo 105

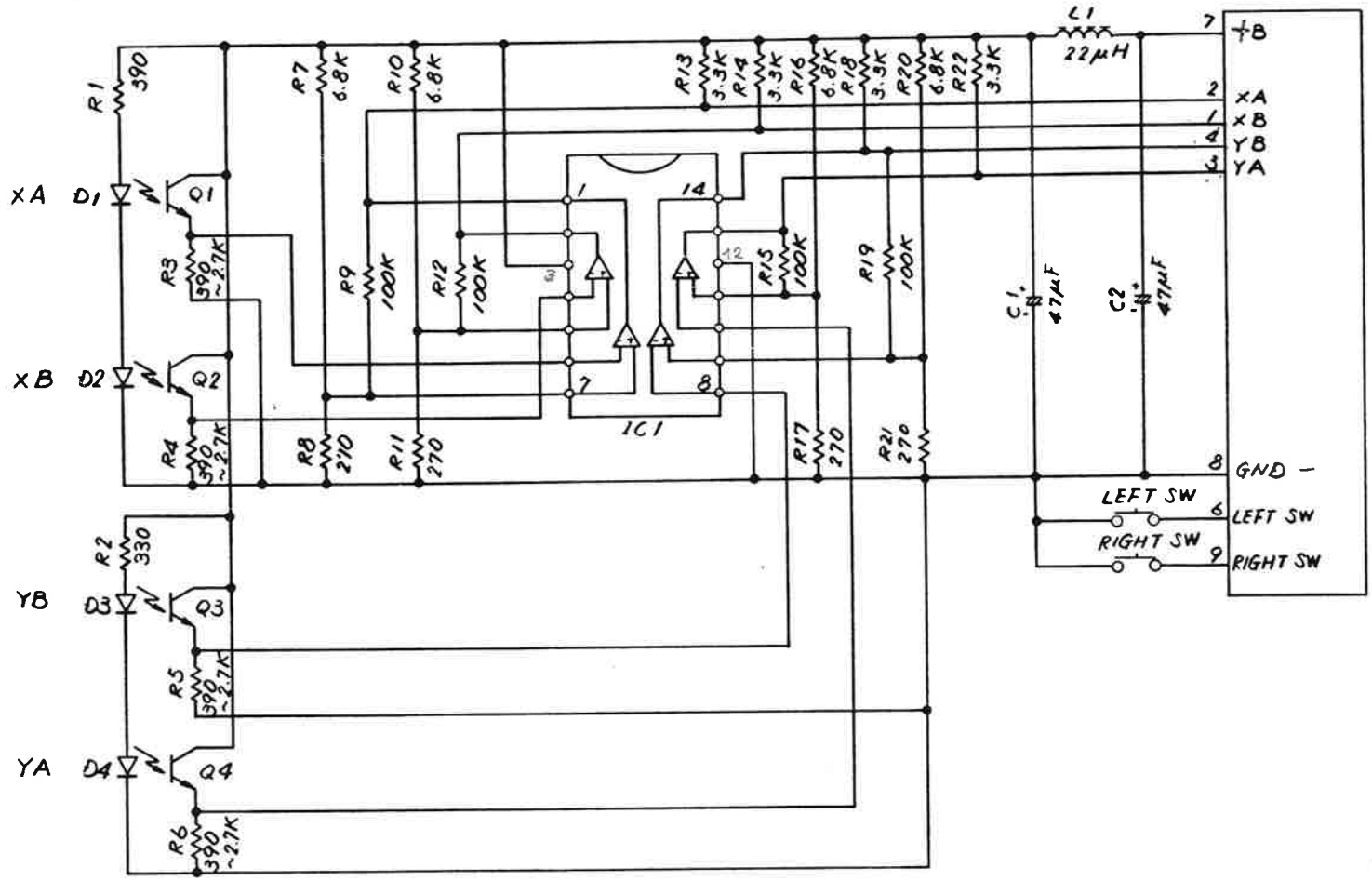
TITLE: SCHEMATIC DIAGRAM (ASP-3-3)

SIZE: B | DRAWING NO: HARD DRIVE | REV: A

SCALE: NONE | SHEET 1 OF 1

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	7/9/87	



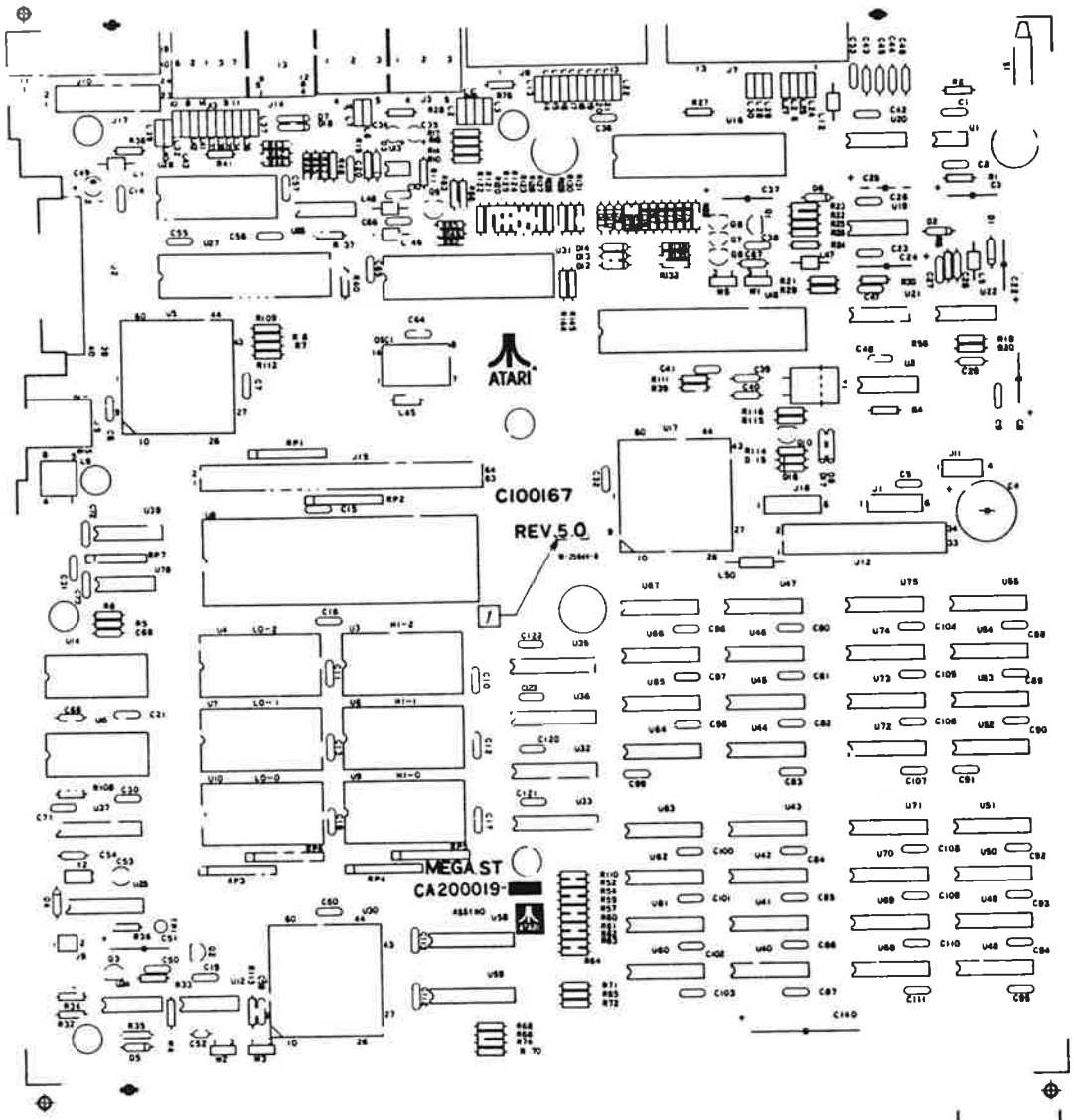
3. IC1 : μPC339G OR TA75339F OR EQUIVALENT
2. Q1~Q4 : PHOTO TRANSISTOR LTR301 OR EQUIVALENT.
1. D1~D4 : LED LTE-301 OR EQUIVALENT.

NOTES - UNLESS OTHERWISE SPECIFIED:

USED ON: STM1	DRAWN BY: H. Kawamata 5-28-85	ATARI (JAPAN) CORPORATION
NEXT ASSY:	CHECKED: K. Kitagawa 9-17-86	Toranomon Kiyoshi Building 3F
MATERIAL:	ENGINEER: A. Shinagawa 10-7-86	4-3-10, Toranomon Minato-ku, Tokyo 105
FINISH:	APPROVED: S. Otaki 10/14/86	TITLE: SCHEMATIC DIAGRAM (MOUSE)
	APPROVED: 10/15/86	SIZE: B; DRAWING NO.; REV: A
		SCALE: NONE; SHEET 1 OF 1

THIRD ANGLE SYSTEM DIMENSION mm

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



SILK PRINT

NOTES—UNLESS OTHERWISE SPECIFIED

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY NTakamura DATE 6.15.87

CHECKED DATE

ENGINEER DATE

APPROVED DATE

APPROVED DATE

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4 3 10, Toranomon Minato-ku, Tokyo 105

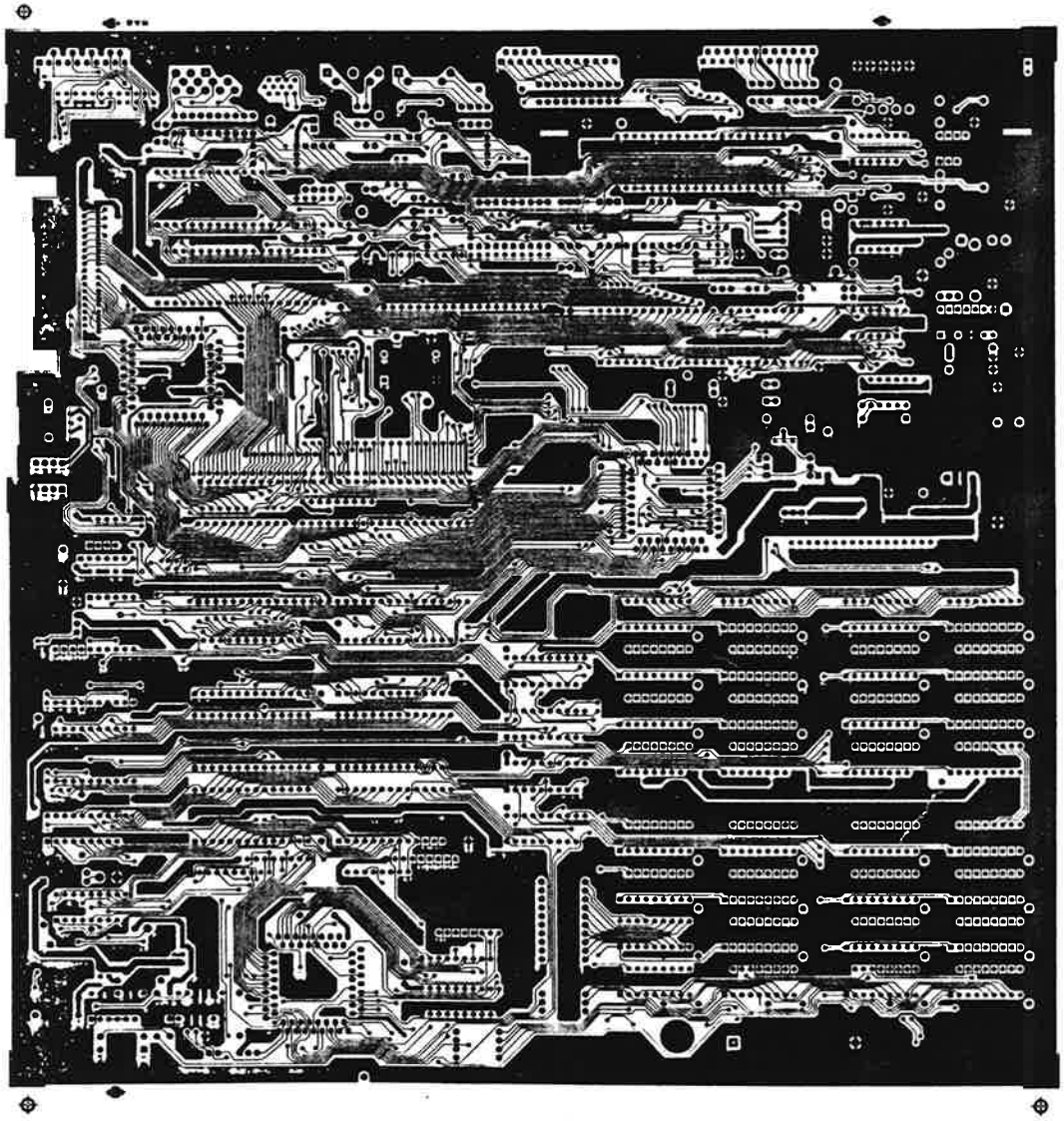
TITLE PCB MEGA

SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 2 OF 6

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



COMPONENT SIDE

NOTES—UNLESS OTHERWISE SPECIFIED:

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY N. Kawamura DATE 6.15.87

CHECKED DATE

ENGINEER DATE

APPROVED DATE

APPROVED DATE

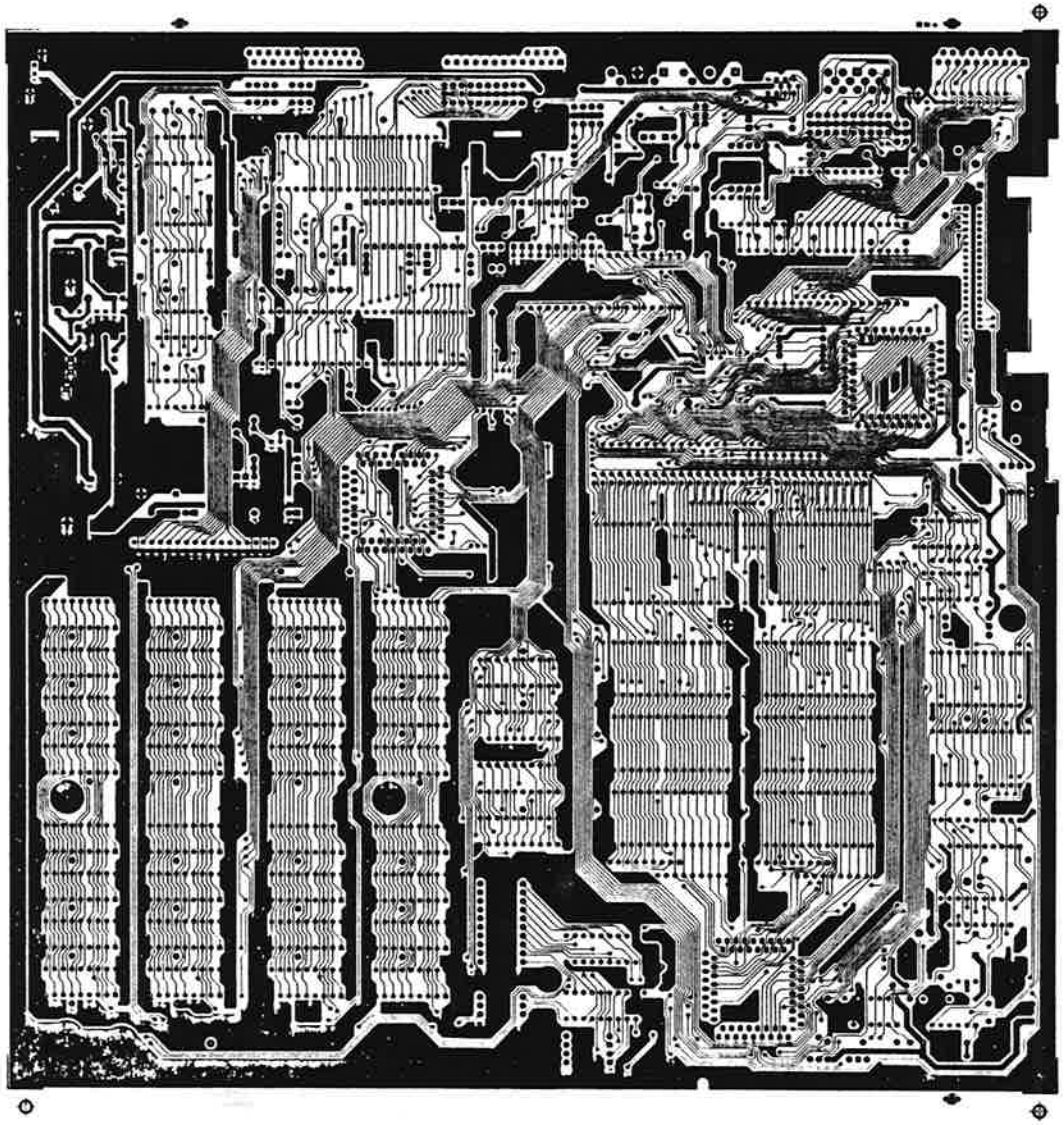
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4 3 10, Toranomon Minato ku Tokyo 105

TITLE PCB MEGA

SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 3 OF 6

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



SOLDER SIDE

NOTES—UNLESS OTHERWISE SPECIFIED

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY N.Hamada DATE 6.13.87

CHECKED DATE

ENGINEER DATE

APPROVED DATE

APPROVED DATE

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4 3 10, Toranomon Minato ku Tokyo 105

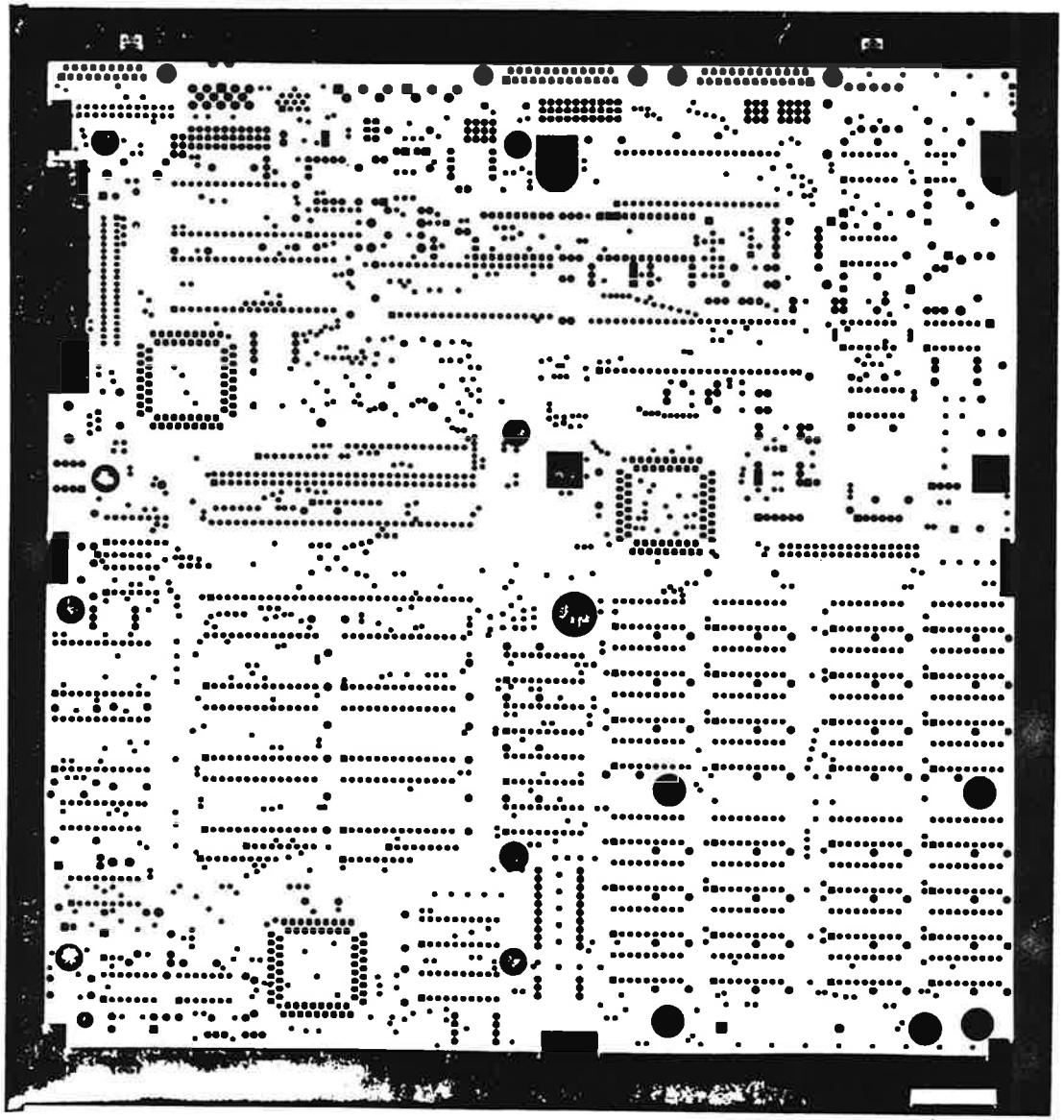
TITLE PCB MEGA

SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 4 OF 6

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



SOLDER MASK
COMPONENT SIDE

NOTES – UNLESS OTHERWISE SPECIFIED

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY N. Kimura DATE 6/15/87
CHECKED DATE
ENGINEER DATE
APPROVED DATE
APPROVED DATE 7/10/87

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4-3-10, Toranomon Minato-ku, Tokyo 105

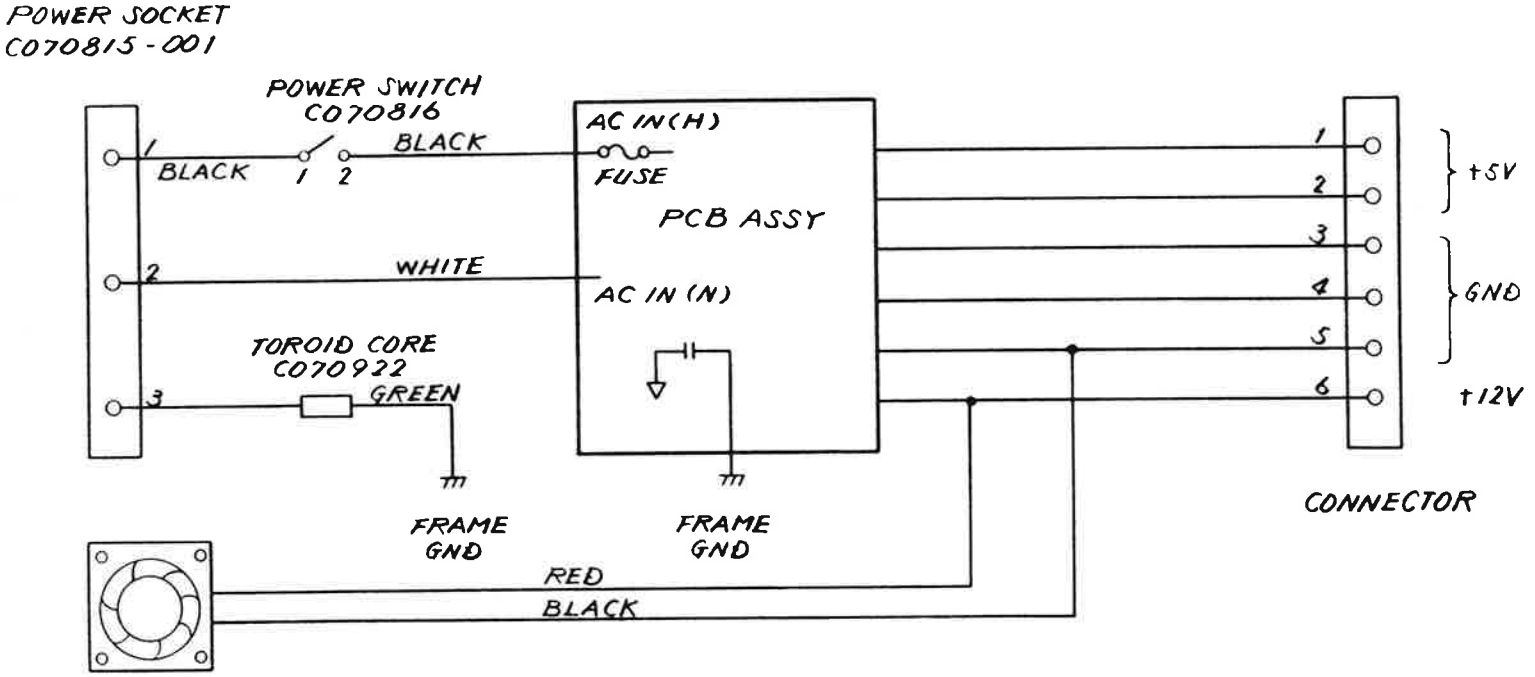
TITLE PCB MEGA

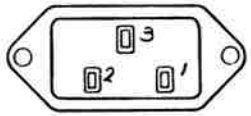
SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 5 OF 6

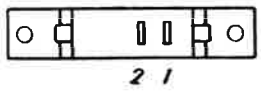
THIRD ANGLE SYSTEM

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		

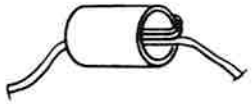




POWER SOCKET
(REAR VIEW)



POWER SWITCH
(REAR VIEW)



TOROID CORE WIRING
3 TURNS

NOTES—UNLESS OTHERWISE SPECIFIED:

NEXT ASSY	USED ON
	ASP34-1

APPLICATION

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

	DRAWN BY	DATE
	H.Kamamoto	2-4-87
CHECKED		DATE
ENGINEER		DATE
APPROVED	A.Shinagawa	2-20-87
APPROVED	N. OKAZAKI	2/20/87

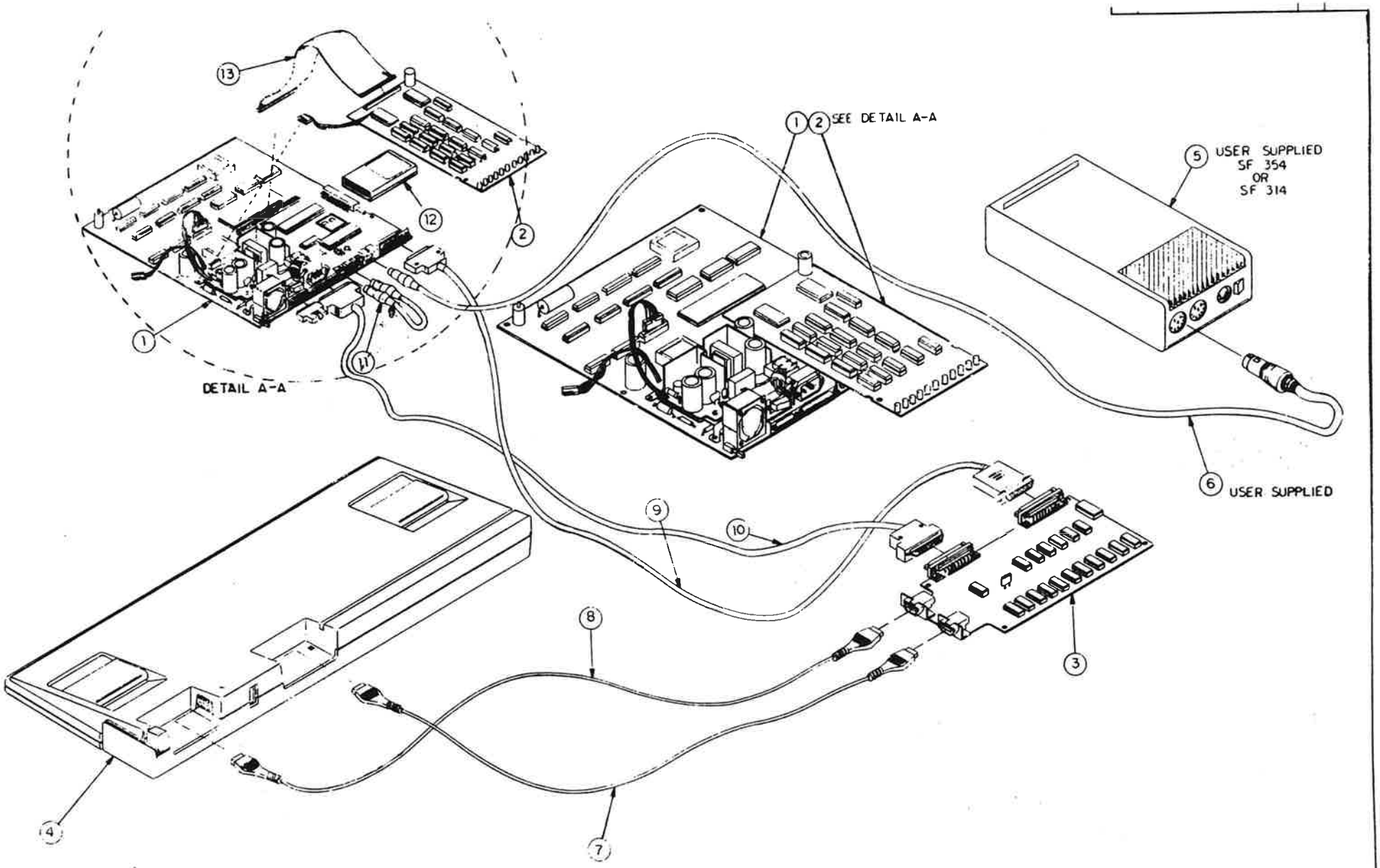
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4-3-10, Toranomon Minato-ku, Tokyo 105

TITLE: POWER SUPPLY ASSY
ASP34-1 (117V)

SIZE B | DRAWING NO | REV B

SCALE NONE | SHEET 5 OF 5

THIRD ANGLE SYSTEM DIMENSION mm



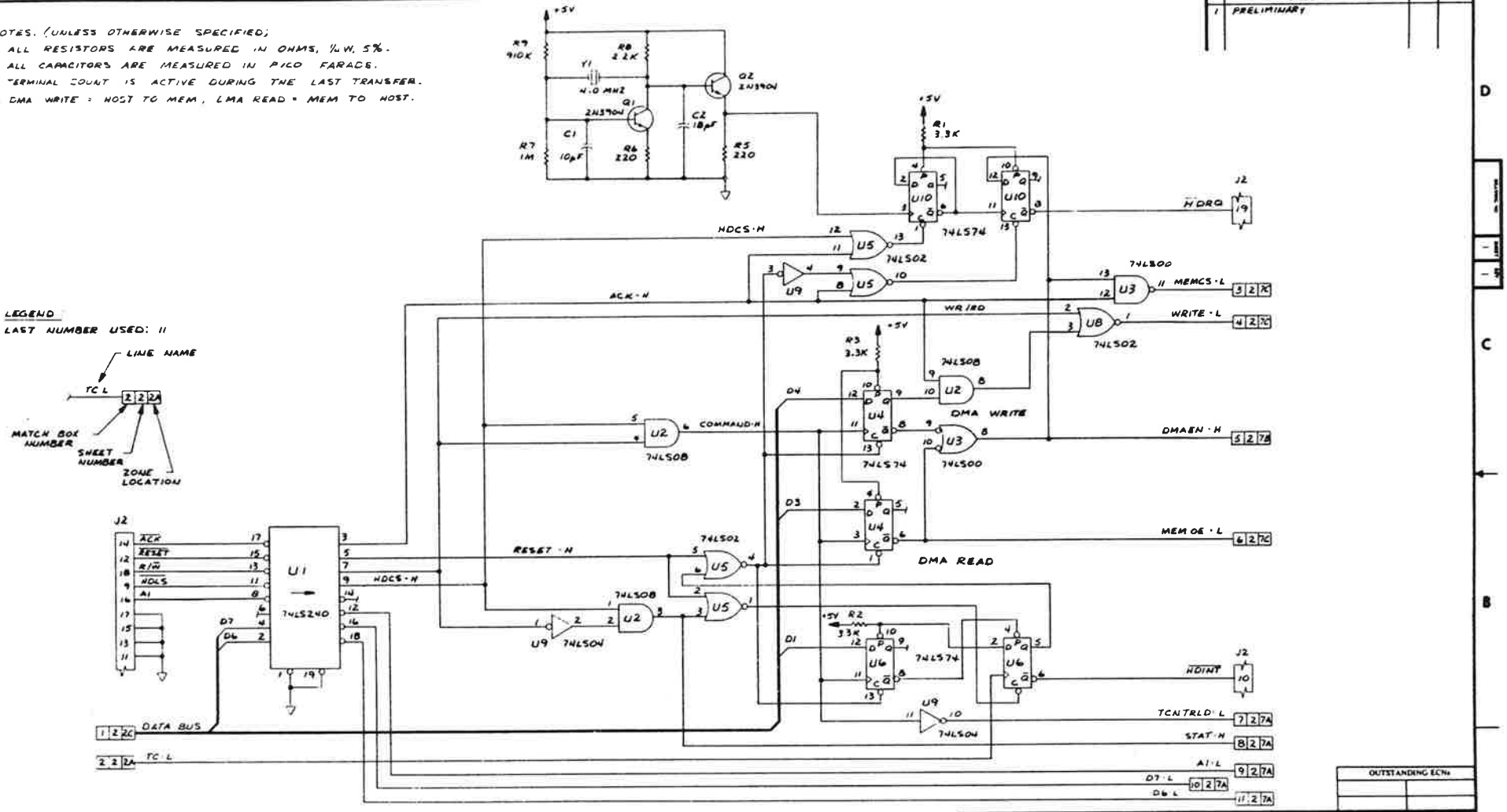
	DRAWN BY Ram 10/13/87	ATARI	ATARI JAPAN CORPORATION
	CHECKED		TITLE ASSY MEGA DIAGNOSTICS
	ENGINEER		SIZE D
	APPROVED		SCALE NONE
	APPROVED		SHEET 1 OF 2

NOTES. (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE MEASURED IN OHMS, ¼ W. 5%.
2. ALL CAPACITORS ARE MEASURED IN PICO FARADS.
3. TERMINAL COUNT IS ACTIVE DURING THE LAST TRANSFER.
4. DMA WRITE = HOST TO MEM, DMA READ = MEM TO HOST.

1	PRELIMINARY		

LEGEND
LAST NUMBER USED: 11

LINE NAME
TC L 2 2 2A
MATCH BOX NUMBER
SHEET NUMBER
ZONE LOCATION



LAST REFERENCE DESIGNATOR USED
U2 R9 C2 Q2 Y1 11
REFERENCE DESIGNATORS NOT USED
U4 R8 11 Y1 Q2

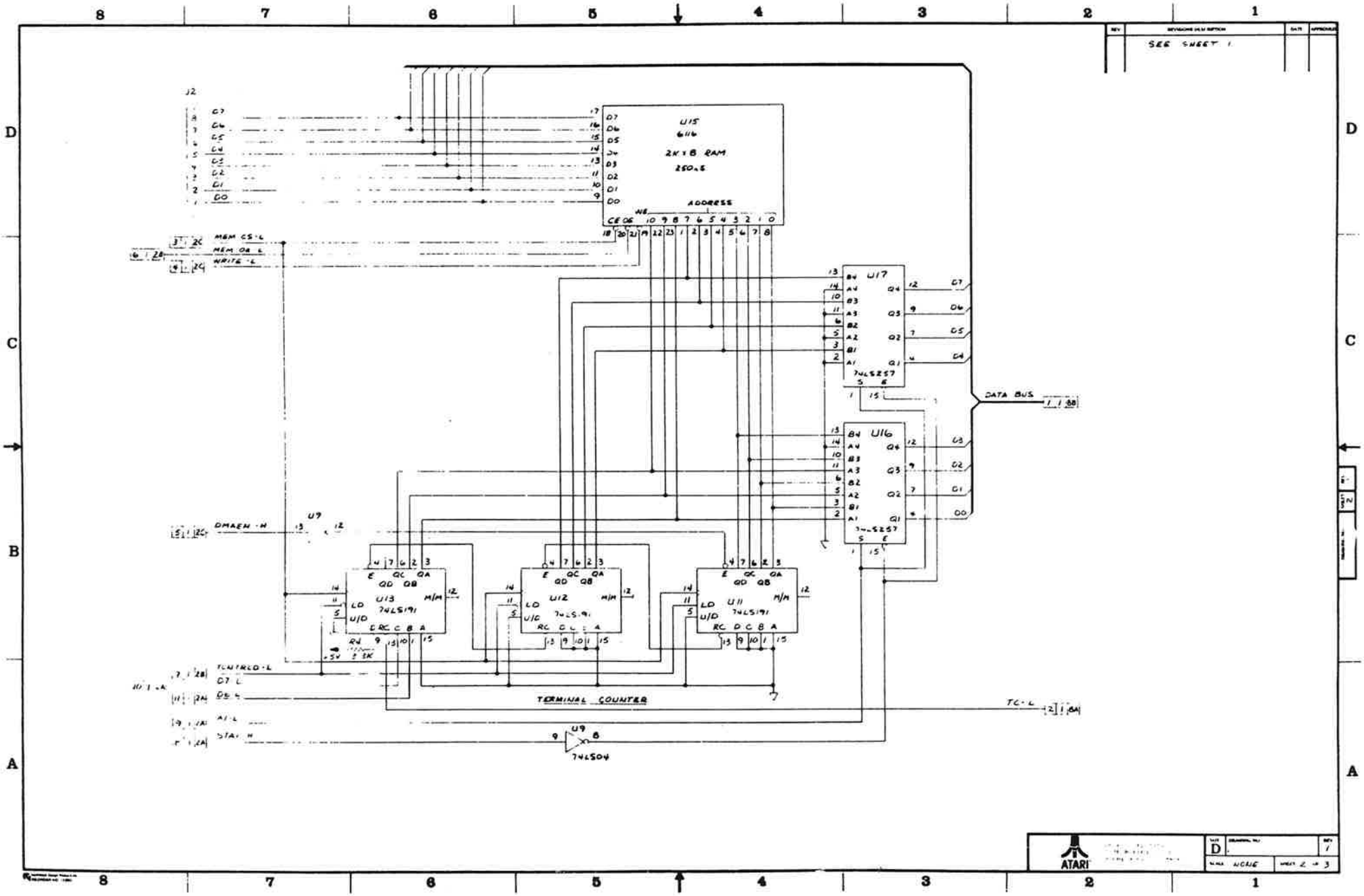
OUTSTANDING ECNs

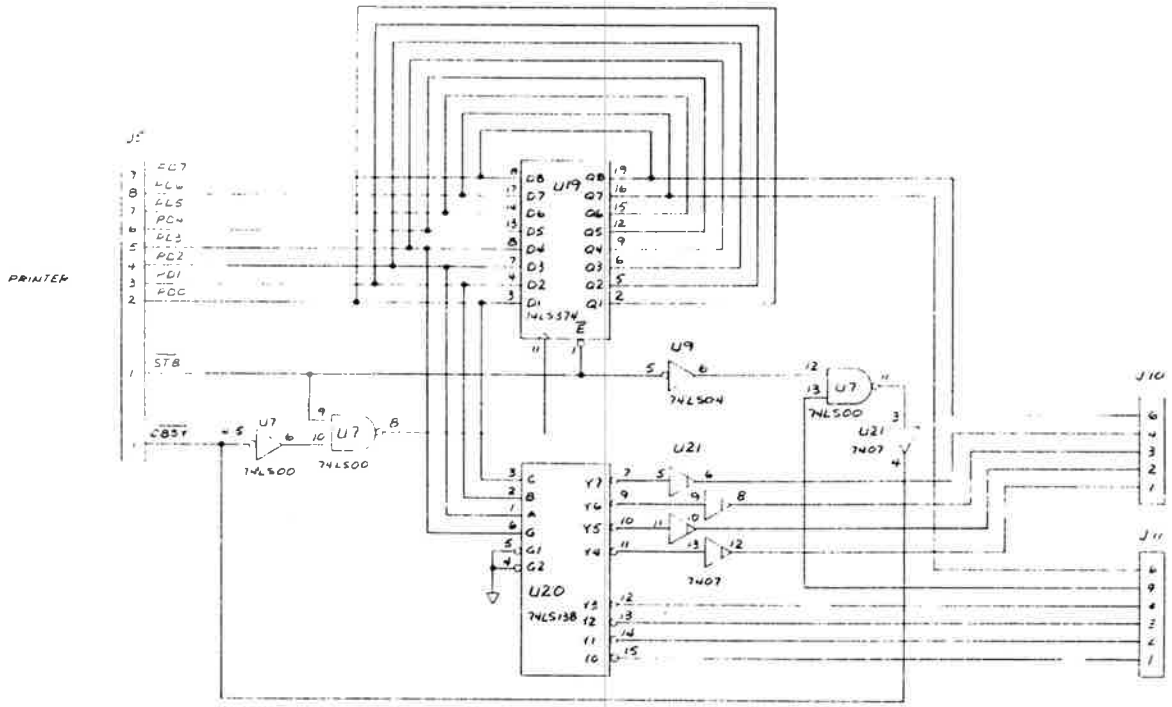
DO NOT SCALE DRAWING

ATARI

TITLE SCHEMATIC
DMA TESTER

SIZE D | DRAWING NO | REV 1
SCALE NONE | SHEET 1 OF 2


SEE SHEET 1
J2
U15
6116
2K x 8 RAM
250nS
ADDRESS
MEM CS-L
MEM OE-L
WRITE-L
U17
U16
74LS257
DATA BUS
U9
DMAEN-H
U13
U12
U11
74LS191
M/M
LD
U/D
RC
CONTROL-L
D7-L
D6-L
A1-L
STAT-H
TERMINAL COUNTER
TC-L
U9
74LS04
ATARI



JOYSTICK AND PRINTER
TEST FIXTURE

SEE SHEET 1

OUTSTANDING ECNs

DO NOT SCALE DRAWING

ATARI

SCHEMATIC
DMA TESTER

SIZE D

NONE

SHEET 3 OF 3

SECTION NINE
GLOSSARY OF PART NAMES AND TERMS

BITBLiT--Atari graphic chip which is actually a DMA device. It is used to transfer block of memory from a source to destination with the patterns and a combination of any logical operations between source and destination which was set up prior to the transfer.

BUS ERROR--Glue has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.

CPU--the 68000 microprocessor.

DMA--direct memory access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, takes place independent of the CPU, so the CPU can be processing while DMA is taking place. Glue arbitrates the bus between the CPU and DMA.

DMA CONTROLLER--Atari proprietary chip which controls the DMA process. All disk I/O goes through this device.

EXCEPTION--a state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also Section Two, System Errors, or a 68000 reference for more detail.

GLUE--Atari proprietary chip which ties together all system timing and control signals.

HALT--state in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bi-directional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert HALT.

HSYNC--timing signal for the video display. Determines when the horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) also is encoded onto IPL1,2 as an interrupt to the CPU.

INTERRUPT--a request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities: the highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and Glue.

MEMORY CONTROLLER--Atari proprietary chip which handles all RAM accesses. See Theory of Operation, Main System and Video Subsystem for details.

MIDI--Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the 1040ST, consists of a 6850 communications chip, driver and receiver chips (74LS04, 74LS05, and PC-900 photocoupler), and an MFP interrupt channel.

MFP--Multi-function Peripheral, also 68901. Interrupt control, timers, and USART for RS232 communication. See Theory of Operation, Main System.

MODULATOR--device which combines video signals R,G,B, VSYNC, and HSYNC into a composite signal for monitors requiring this type input, and also modulates this signal, combined with audio, onto an RF carrier for output to a television.

PHASE LOCKED LOOP--circuit which locks the horizontal sync signal onto the color burst reference frequency for accurate color on the T.V. Without this circuit, colors on the T.V. become unstable, flickering or shifting about on the screen. The PPL may be on a daughter board located in front of the video shield or hand wired onto the main board within the video shield, or (possibly) in later versions, integrated into the printed circuit board.

PSG--Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.

RS232C--Electical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the ST computers, consists of the MFP, PSG, 1488, and 1489 chips.

1772--Western Digital Floppy Disk Controller.

6850--also ACIA (Asynchronous Communication Interface Adapter). Interfaces between 8 bit parallel bus and serial communication bus. In the ST, there are two 6850s, one for keyboard communication, and one for MIDI communication.

68901--see MFP.

SUPERVISOR MODE--state of the CPU in which it is allowed to access all hardware and RAM locations, and perform some priviliged instructions. Determined by the state of a bit in the Status Register. The operating system operates in supervisor mode, and switches to user mode before passing control to an application (although the application can enter supervisor mode if it wishes).

USER MODE--state of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.

VSYNC--signal used for vertical synchronization of CRT display device. Occurs at 70 Hz (monochrome), or 50 or 60 Hz color.

YM2149--see PSG.