ATARI ®

MegaSTe ®

Service

Manual

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MEGASTE DIAGNOSTIC MANUAL RELEASE NOTES

This is the first release of the MegaSTe Diagnostic Manual. At the time it was produced the Main PCB Assembly drawing (IPB) and the Test Configuration Setup drawing were not available. Photocopies of these drawings have been provided in the meantime until the actual drawings are complete. The new drawings will then be sent to each subsidiary to replace the existing photocopies.

CONTENTS

SECTION ONE

INTRODUCTION

1.1 OVERVIEW

The Atari MegaSTe® is the newest enhancement in the series of Atari ST® computers. The MegaSTe® is upward compatible with the Atari STe® and is designed as an integrated unit with processor, memory, and I/O, floppy disk drive, and power supply in one package. The MegaSTe® provides either 1, 2, or 4 Mbytes of RAM memory and 256 Kbytes of ROM memory. A 16 Kbyte cache memory is also provided. The floppy disk drive storage capacity is 720 Kbyte (formatted). An optional 1.44 Mbyte (formatted) floppy, hard disk drive, and floating point coprocessor can also be added.

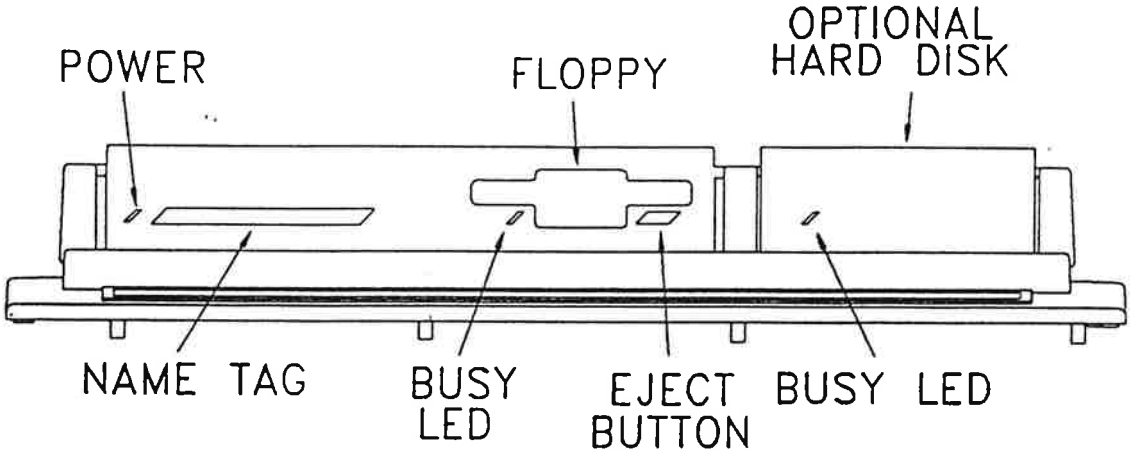
1.2 MAIN COMPONENTS

MAIN BOARD

- Power Supply
- Floppy Disk Drive
- Optional Hard Disk Drive
- Keyboard
- Mouse
- Plastic Case (upper and lower)

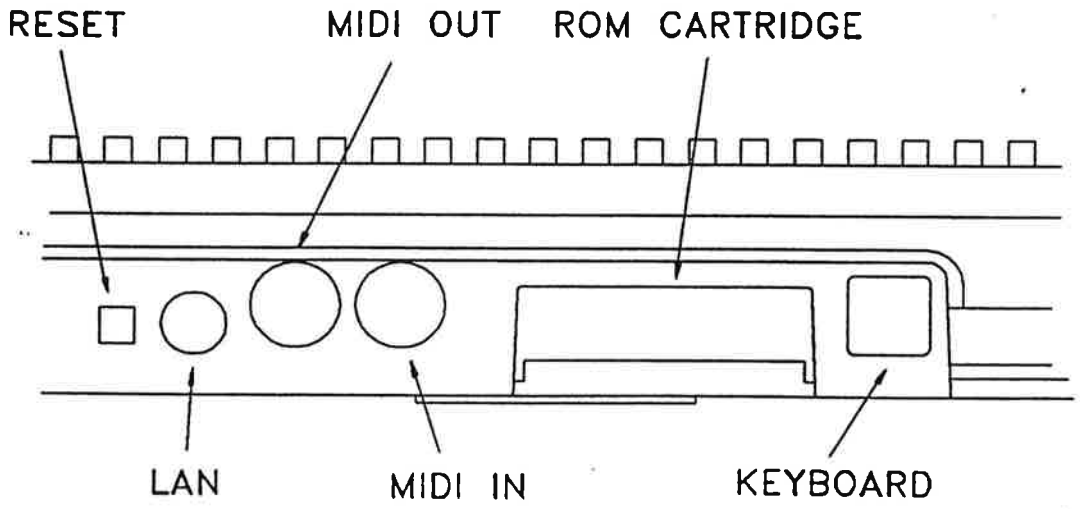
1.3 CASE DESIGN

The front of the MegaSTe® contains the floppy disk drive with an eject button and busy LED. An optional hard disk can also be installed and contains its own busy LED.



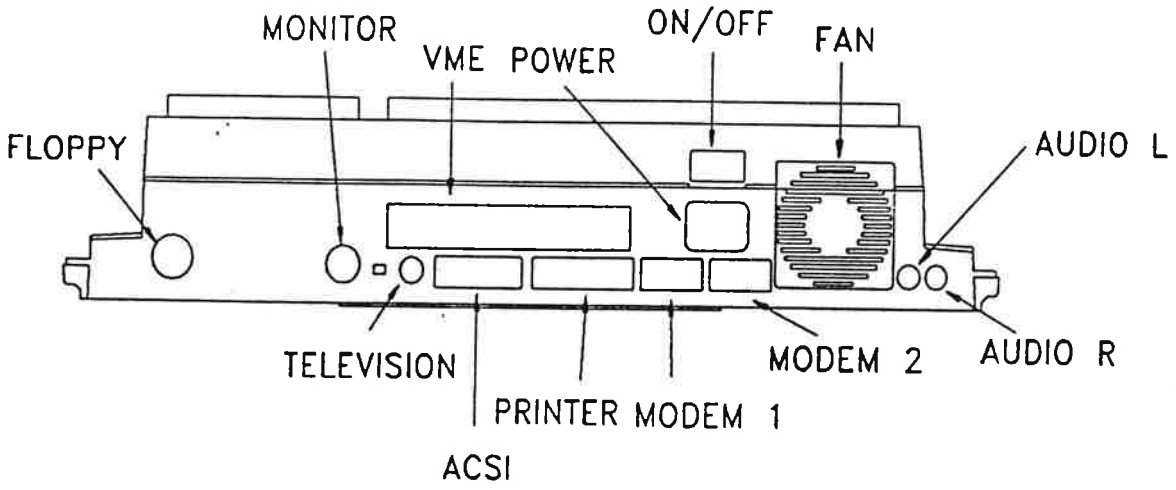
FRONT VIEW

The left side of the MegaSTe® case contains the following items from left to right. Reset button, LAN connector, MIDI out jack, MIDI in jack, ROM cartridge port, and keyboard jack.



LEFT SIDE VIEW

The rear of the MegaSTe® contains the following items from left to right. External floppy jack, monitor jack, TV jack, Serial 2 or VME slot, external ACSI interface connector, printer connector, modem 1 connector, on/off switch, power plug, modem 2 connector, fan, audio R connector, and audio L connector.



REAR VIEW

1.4 POWER SUPPLY

1.4.1 POWER SUPPLY RATING

The MegaSTe® has an integral switching power supply providing 65 watts of power. The supply can accept AC input of 100-240VAC at 2A, 50/60Hz. The power supply provides the following voltages and currents to the system:

Voltage	Current
+5V	7A
-5V	2A
+12V	0.4A
-12V	0.3A

SECTION TWO

THEORY OF OPERATION

2.1 OVERVIEW

The MegaSTe® is an upward compatible extension of the Atari ST® architecture. A VME bus has been included in the MegaSTe® for expansion. The hardware is composed of a main system (central processing unit and support chips), audio/video subsystem, and several I/O subsystems.

Main System

- MC68000 processor running at 8/16 MHz
- Optional MC68881 or MC68882 coprocessor
- 256 Kbytes of ROM
- 1024, 2048 or 4096 Kbytes of RAM
- 16 Kbytes of cache RAM
- Processor speed/cache control
- Interrupt mask, status, and control (MFP and SCU)
- System timing and Bus control (GSTMCU, PALs U3, U6, U2)
- DMA support
- Battery backed-up Real-time clock

Audio/Video Subsystem

- Bit Mapped video display using 32 Kbytes of RAM relocatable anywhere in memory. Three available display modes:

  1. 320 X 200 16 out of 4096 colors
  2. 640 X 200 4 out of 4096 colors
  3. 640 X 400 monochrome

- Monitor interfaces include:
  1. RGB
  2. Monochrome
  3. Composite
  4. Television

- Audio outputs:
  1. Programmable sound generator.
  2. DMA sound output

I/O Subsystems

- Floppy disk interface
- High-speed serial ports
- MFP serial port
- Parallel printer interface
- Intelligent keyboard interface
- Mouse and Joystick interface
- Hard disk interface
- Musical Instrument Digital Interface (MIDI)
- VME bus

2.2 MAIN SYSTEM

The hardware contained in the main system of the Atari MegaSTe® are the processor, optional coprocessor, ROM, RAM, cache RAM, system speed and cache control, Interrupt control (SCU and MFP), Timing and Bus control (GSTMCU), DMA support, Real-time clock, and ACSI interface.

2.2.1 PROCESSOR U007 PG. 1

The processor used in the Atari MegaSTe® system is a 16 MHz Motorola® MC68000 with a 32-bit internal architecture, 16-bit external data bus, and a 24-bit address bus. The processor can be operated at either 8 or 16 MHz.

2.2.2 COPROCESSOR (OPTIONAL) UB02 PG. 11

A socket is provided in the MegaSTe® for an optional Motorola® MC68881 or high performance MC68882 floating point coprocessor. The coprocessor is clocked at 16 MHz independent of the speed at which the processor is running. The processor does not directly support the coprocessor but accesses it as an I/O device with memory type instructions via its address and data buses.

2.2.2.1 COPROCESSOR CONTROL SIGNAL GENERATION UB01 PG. 11

Chip select and data strobe signals for the coprocessor are generated by a PAL in location UB01.

2.2.3 ROM U206, U207 PG. 2

The system contains two 128 Kbyte ROMs for a total of 256 Kbyte of access space. Since system bus access is 16-bits wide, both ROMs must be present for proper operation. Included in the tasks the ROM performs is system initialization and boot code from the floppy, hard disk, ACSI interface, and network. The ROM also contains a language specific implementation of the TOS operating system.

2.2.4 RAM U701, U702, U703, U704 PG. 7

The MegaSTe® includes either 1, 2, or 4 Mbytes of RAM used for both system and video. The RAM is implemented with 8-bit SIMMs (Single Inline Memory Module) and must be installed in matching pairs. Memory accesses to the RAM are interleaved between the Memory Controller and the Video Controller in 250ns time slices. During display cycles, the processor is prevented from accessing the RAM. However, the processor will be allotted the next 250ns time slice.

Additional memory can be installed in the system via VME memory cards. Up to 4 Mbytes of additional 16-bit wide RAM can be installed in this way. VME memory will typically run slower than on-board system memory because all accesses incur an additional wait state.

RAM memory map:

Address	Usage
000008 - 000800	System memory (privileged access)
000800 - 07FFFF	Low Bank (1 Mbyte systems)
080000 - 0FFFFF	High Bank (1 Mbyte systems)
000800 - 0FFFFF	Low Bank (2 Mbyte systems)
100000 - 1FFFFF	High Bank (2 Mbyte systems)
000800 - 1FFFFF	Low bank (4 Mbyte systems)
1FFFFF - 3FFFFF	High bank (4 Mbyte systems)

2.2.5 CACHE RAM U004, U005, U008, U009 PG. 1

Cache RAM consists of 16 Kbytes of fast SRAM memory. RAM cycles are cached using 8K words, which are 16-bits wide. This permits cache-hit memory cycles to run at zero wait states and without taking a cycle on the system bus when the processor is running at 16 MHz.

2.2.6 SYSTEM CONTROL UNIT (SCU) U801 PG. 8

The SCU provides several system support functions including interrupt masking and status reporting, interrupt generation, and bus timeout detection.

2.2.6.1 INTERRUPT MASK AND CURRENT STATUS

The SCU contains two registers used to mask interrupts to the processor. These registers, in effect, screen the interrupts from both main system devices and VME bus devices and present them, when enabled (not masked), to the processor. Masked interrupts (not enabled) are not presented and therefore not seen by the processor. These registers are cleared at power up or reset, disabling all interrupts.

The SCU also contains a register which latches the current state of the seven interrupt request levels from each one of the sources. This register shows the state of the interrupt lines before they are ANDed with the mask registers.

2.2.6.2 INTERRUPT GENERATION

The system can write to an I/O address to generate a level 1 autovectored interrupt to the processor. The SCU is hardwired to the following interrupt scheme:

- Only interrupt levels 5 and 6 have external interrupt acknowledge (IACK) pins and are capable of generating vectored interrupts to the system.
- SCU generated interrupts IRQ1 and IRQ3 are hardwired to the corresponding priorities and are always autovectored.
- The VMEbus ACFAIL generates an IRQ7 interrupt to the processor. The only other source of IRQ7 interrupt is from a VMEbus card.

2.2.6.3 BUS TIMER

The SCU implements a bus timer so that if a bus cycle is not terminated within 16us, the SCU will generate a bus error signal.

2.2.6.4 PROCESSOR/CACHE CONTROL

There is a register implemented in the SCU used to select processor speed (8/16 MHz) and enable cache memory. The address decode for the register is done by PAL UA02 (Pg. 10). Bit 0 enables the cache and bit 1 selects the processor speed. The clock control signal is generated by PAL U407 (Pg. 4) and supplied to PAL U11 (Pg. 1). The cache enable signal is also supplied to PAL U11. These signals are the multiplexed to the processor clock pin and cache enable pins of the SRAM by PAL U12 (Pg. 1).

2.2.7 68901 MFP U306 PG. 3

2.2.7.1 MFP INTERRUPT CONTROL

The 68901 MFP handles up to 16 interrupts. Currently all but one are used. Each interrupt can be masked off or disabled by programming the MFP. The 8 inputs are also directly readable by the CPU. When the MFP receives an interrupt input, or generates an input internally, if the interrupt is enabled, MPINT will be driven low. When the CPU is ready to respond, it signals interrupt acknowledge (PC0-PC2 high and VMA low) and GSTMCU will assert IACK (interrupt acknowledge). The MFP will assert DTACK and put a vector number on the data bus, which the CPU will read and use to calculate the address of the interrupt routine.

The interrupts controlled by the MFP are: monochrome monitor detect (MONOMON), RS-232 (Including CTS, DCD, and RI), floppy and hard disk (FDINT and HDINT respectively), parallel port BUSY, display enable (DE, which equals the start of the display line), 6850 IRQ's for keyboard and MIDI data, and MFP timers.

Not all I/O operations are interrupts. The CPU can also poll the MFP while waiting for an operation to complete. The MFP also contains four timers. These are used by the Operating System for event timing and by the RS-232 port for transmit and receive clocks.

2.2.8 SYSTEM TIMING AND BUS CONTROL GSTMCU U501 PG. 5 PALS U2, U3, AND U6 PG. 11

The GSTMCU is an integral part of the system and is involved in almost every operation in the computer. The functions performed by the GSTMCU include clock dividers, video timing, signal and bus arbitration, memory control, and chip selects.

2.2.8.1 CLOCK DIVIDERS

The clock dividers within the GSTMCU are used to take the 16 MHz input and divide it into 4 MHz, 8 MHz, and 500 kHz clocks for use by other devices in the system.

2.2.8.2 VIDEO TIMING

The GSTMCU outputs the signals BLANK, DE (Display Enable), VSYNC, and HSYNC to generate system video. There is also a read/write register within the GSTMCU which is used to configure for 50, 60, or 71 Hz monitor operation (done by software).

2.2.8.3 SIGNAL AND BUS ARBITRATION

The GSTMCU arbitrates the bus during DMA cycles to prevent the processor and DMA controller from interfering with one another. PAL U6 synchronizes the bus error and data transfer acknowledge signals to the processor. PAL U3 is a data strobe state machine used to generate both upper and lower data strobes on byte reads when cache RAM is enabled. PAL U2 is used to latch latch data strobe, address strobe, and read/write signals to the processor.

2.2.8.4 MEMORY CONTROL

The GSTMCU takes addresses from the address bus and coverts them to Row Address Strobe (RAS) and Column Address Strobe (CAS) signals to control all RAM accesses. The Memory Controller internal to this device is also responsible for refreshing the DRAM (dynamic RAM), loading the Video Shifter with display data, and sending or receiving data during DMA cycles.

2.2.8.5 CHIP SELECTS

The GSTMCU decodes addresses and generates chip selects to the 6850's, 68901 MFP, DMA Controller, Programmable Sound Generator, internal Memory Controller, and ROMs. It receives signals from the MFP, DMA, and Memory Controller to synchronize data transfers. The GSTMCU also decodes the addresses necessary to enable the RAM and ROM.

2.2.9 DMA SUPPORT U404 PG. 4

Direct memory access is provided to support both low speed (250 to 500 kilobits/sec) and high speed (up to 8 Megabits/sec) 8-bit device controllers. The floppy disk transfers at low speed and the hard disk (or other devices on the hard disk port) transfer at high speed.

For DMA to take place, the Memory Controller is given the address of where to take data from or put data in RAM, the DMA Controller is set up (with channel, high or low speed, and how many bytes) and the peripheral is given a command to send or receive data.

The entire block of data (the size must be given to the DMA Controller and the peripheral before the operation starts) is then transferred to or from memory without intervention by the CPU.

2.2.10 REAL-TIME CLOCK U402 PG. 4

The MegaSTe® system includes a Real-time Clock chip. When the system is powered on the real-time clock is powered by the main PCB power supply. In the event of a power failure, or when the system is powered off, the real-time clock is powered by a 3.6v lithium battery. This allows the date and time to be maintained even when there is no power to the unit.

The real-time clock provides time of day (down to one second resolution) and date. The RTC is provided with a 32.760 kHz oscillator that is independent of all other system clocks.

The chip is accessed through 32 4-bit registers accessed in two banks. Bank 0 allows reading and setting of each digit of the date and time. It also allows access to test and control registers within the device. Bank 1 allows setting the digits of the alarm function and controls the mode of operation of the clock.

2.3 AUDIO/VIDEO SUBSYSTEM

2.3.1 VIDEO SUBSYSTEM U501, U502, U205, U503 PG. 5

The video subsystem consists of the video display memory (an arbitrary block of RAM starting on any word boundary), the GSTMCU U501, a graphics control chip GSTSHFTR U502, a graphics coprocessor chip STB U205, some discrete components to drive the video output, and an RF modulator U503. The role of the GSTMCU has already been covered in section 2.2.8.2

2.3.1.1 GSTSHFTR VIDEO SHIFTER U502 PG. 5

There are 16 color palette registers in the shifter. All 16 may be used in low resolution (320 X 200). Four may be used in medium resolution (640 X 200), and one may be used in monochrome (640 X 400) high resolution (actually only bit 0 of register 0 is used for inverse/normal video). Contained in each entry are twelve-bits of color; four-bits each for red, green, and blue. Therefore there are 16 X 16 X 16 or 4096 colors possible for each entry. For a given pixel, the color which is displayed is taken from the palette referred to by getting information from each logical plane (see the description of video display in section 2.3.1.3). The shifter will output the red, blue, and green levels specified by that palette.

Note that there are four outputs for each color. Each output is either on or off. This makes the number of possible output levels 2 to the 4th power or 16. The four outputs are summed through a resistor network to proportion the voltage level to give sixteen equal steps. In monochrome mode, the color palettes are bypassed and there is a separate output.

2.3.1.2 GRAPHICS COPROCESSOR STB U205 PG. 2

The graphics coprocessor (Blitter) handles the extra burden of graphics video generation on the processor. The STB performs bit aligned block transfers required in graphics generation, adding to the capability of the processor which only works on word or byte boundaries. The STB also provides barrel shift functions that are not contained in the processor.

2.3.1.3 VIDEO DISPLAY MEMORY

Display memory is part of main memory with the physical screen origin located at the top left corner of the screen. Display memory is configured as 1, 2, or 4 logical planes interwoven by 16-bit words into contiguous memory to form one 32,000 byte physical plane starting at any 2-byte boundary. The starting address of display memory is placed in the Memory Controller's Video Base High, Video Base Mid, and Video Base Low registers by the Operating System or application. This register is loaded into the Video Address counter (high, mid, and low) at the beginning of each frame. The address counter is incremented as the Bit Map planes are read.

The Memory Controller will load display information into the Video Shifter 16 bits at a time, and the Video Shifter will decode this information to generate a serial display stream. In monochrome mode, each bit represents one pixel on or off. In color, bits are combined from each plane to generate the correct level of red, green, and blue.

For example, in low resolution (4 planes) four words are loaded into the Video Shifter for each word (16 pixels) displayed on the screen. The Video Shifter combines bit 0 from each word to form a four bit number (0-15), and takes the color from the palette referenced by that number (e.g. 0101 = 5, use color from palette register 5) and outputs those levels, then takes bit 1 from each plane and outputs the color from the palette referenced by those four bits, etc.

2.3.1.4 TELEVISION INTERFACE PG. 5

The MC1377 takes the red, green, and blue video signals from the emitter followers Q501, Q502, and Q503 and adds them to the HSYNC and VSYNC signals to form composite video. The composite signal is then modulated onto an RF carrier and locked onto the color burst frequency by a phase locked loop. The RF video is then output to an RCA type jack on the back of the computer.

2.3.1.5 HORIZONTAL SCROLLING

Two additional registers implement a horizontal smooth scroll capability. The horizontal pixel scroll register holds a pixel offset value from 0-15 at which to begin display. Increasing this value by one will scroll the whole display one pixel to the left. The extra line width register contains a number of words that is added to the ending address of each display line to get the beginning address of the next display line. It puts an undisplayed area to the right of the video screen. By using these two registers the video screen can be used as a horizontally scrolling window.

2.3.1.6 GENLOCK AND THE MEGASTE®

The MegaSTe® has the ability to accept external sync. This was done to allow synchronization of the MegaSTe® video with an external source. In order to do this reliably, the system clock must also be phase-locked to the input sync signal. To do this pin three of the monitor connector must be grounded. The clock can then be input on pin four of the monitor connector. The internal frequency of this clock is 32.215905 MHz for NTSC and 32.084988 MHz for PAL.

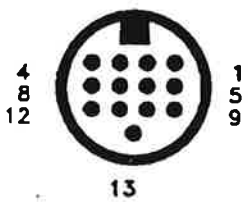
2.3.1.7 MONITOR INPUT LEVELS

HSYNC - TTL level, negative, 3.3 K ohm
VSYNC - TTL level, negative, 3.3 K ohm
Monochrome - digital 1.0V p-p, 75 ohm
RGB - analog 0-1.0V p-p, 75 ohm
Audio - 1.0V p-p, 1 K ohm

2.3.1.7 MONITOR CONNECTOR

The video output is provided on a 13-pin DIN type connector located on the back of the computer. The connector is compatible with the ST® and STe® series systems. Either color or monochrome monitors can be used. The pinout of this connector is as follows:

Pin	Function
1	Audio Out
2	Composite Video
3	External Clock Select (Pull low for external clock on pin 4)
4	Monochrome Monitor Detect (When used for GENLOCK becomes clock)
5	Audio Input
6	Green
7	Red
8	Peritel Power
9	HSYNC
10	Blue
11	Monochrome Out
12	VSYNC
13	Ground



2.3.2 AUDIO SUBSYSTEM

The MegaSTe® extends the present audio subsystem of the Atari ST® computer. It mixes the output of the existing ST programmable sound generator (PSG) with a DMA-driven dual channel digital to analog subsystem. The MegaSTe® combines these two sources and sends the resulting audio through the audio output pin of the monitor connector. In addition, the audio output can be connected to an external stereo amplifier for high-fidelity sound.

2.3.2.1 PROGRAMMABLE SOUND GENERATOR U305 PG. 3, U608 PG. 6

The programmable sound generator (U305) produces music synthesis, sound effects, and audio feedback. With an applied clock of 2 MHz, the PSG is capable of providing frequencies from 30 Hz to 112 kHz. The PSG has the ability to perform using three separate voice channels. The three sound channel outputs are mixed together and sent to the LMC1992 volume and tone control chip (U608).

2.3.2.2 DMA SOUND

Sound in the form of digitized samples is stored in the system memory. These samples are fetched from dual purpose memory during horizontal blanking cycles and provided to a Digital to Analog Converter (DAC) at a constant sample frequency specified by the user. The output of the DAC is then low pass filtered to a frequency equal to forty percent of the sample frequency by a four pole switched capacitor low pass filter. The signal is further filtered by a two pole fixed frequency (15 kHz) low pass filter and sent to the LMC1992 Volume and Tone Control chip. The signal is then made available to two RCA type jacks at the back of the computer as well as the audio output pin of the monitor connector.

2.4 I/O SUBSYSTEMS

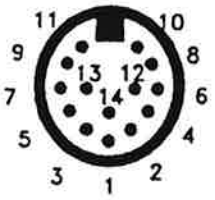
2.4.1 FLOPPY DISK INTERFACE U405 PG. 4

The floppy disk subsystem is designed around the Floppy Disk Controller supporting up to two daisy-chained disk drives. One internal and one external drive can be connected to the system. The subsystem interfaces to the RAM through the ACSI DMA controller. Commands and arguments are sent to the FDC by first writing to the DMA Mode Control Register to select the desired FDC register and then writing the data bytes.

The standard drive for the system is a 720 Kbyte (capacity after formatting) 3 1/2-inch floppy disk. The internal drive cabling supports the Disk Change Line signal from the floppy drive and is read when the drive is selected, and is asserted when power is applied or a diskette is removed from the drive. The signal can be cleared by issuing a step command to the drive. Two clock speeds are provided to support both low and high density floppy drives. The decode for the register that hold the selection id done by PAL UA02 (Pg. 11). The signal is sent to PAL U407 (Pg. 4) where the proper clock is sent to the floppy disk controller.

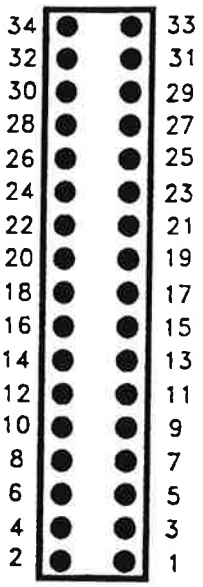
2.4.1.1 FLOPPY PORT PINOUT

Pin	Function
1	Read Data
2	Side 0 Select
3	Logic Ground
4	Index Pulse
5	Drive 0 Select
6	Drive 1 Select
7	Logic Ground
8	Motor On
9	Direction In
10	Step
11	Write Data
12	Write Gate
13	Track 00
14	Write Protect



2.4.1.2 INTERNAL FLOPPY DISK DRIVE CONNECTOR PINOUT

Pin	Function
1-33 Odd	Ground
2	FDDS
4	No Connect
6	No Connect
8	Index
10	Drive 0 Select
12	Drive 1 Select
14	No Connect
16	Motor On
18	Direction In
20	Step
22	Write Data
24	Write Gate
26	Track 00
28	Write Protect
30	Read Data
32	Side 0 Select
34	No Connect



2.4.2 HIGH SPEED SERIAL PORTS SCC UA04 PG 11

The MegaSTe® contains an 85C30 Serial Communications Controller (SCC) that provides a dual channel, multi-protocol device that provides two serial ports. Port A can be used as either a network port or a standard slow speed RS232C serial port. The input/output of port A is routed to the appropriate connector, either an 8-pin mini-DIN or DB-9P, by setting a bit in a register (user application or Operating System). The output pins on the unselected port remain inactive

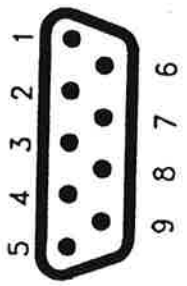
Port B is configured to be a low speed standard RS232C serial port that can be used for connecting a modem or local mainframe. The input/output of Port B is connected to a DB-9P connector and modem control signals are derived directly from the 85C30 Port B control lines. Port B can also operate with split transmit and receive baud rates.

The PCLK input to the SCC is rated at 8 MHz. The RTXCA and RTXCB input is provided with a 1.672 MHz clock. The TRXCA input comes from the LAN connector, and the TRXCB input is rated at 2.4576 MHz. Control signals are sent to the SCC by PAL UA03 (Pg. 11).

2.4.2.1 SCC RS-232 PINOUTS

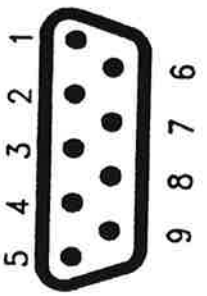
Port A

Pin	Function
1	Carrier Detect (In)
2	Receive Data (In)
3	Transmit Data (Out)
4	Data Terminal Ready (Out)
5	Ground
6	Data Set Ready (In)
7	Request to Send (Out)
8	Clear to Send (In)
9	No Connect



Port B

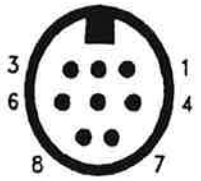
Pin	Function
1	Carrier Detect (In)
2	Receive Data (In)
3	Transmit Data (Out)
4	Data Terminal Ready (Out)
5	Ground
6	Data Set Ready (In)
7	Request to Send (Out)
8	Clear to Send (In)
9	No Connect



2.4.2.2 SCC LAN CONNECTOR PINOUT

Port A LAN Connector

Pin	Function
1	Output Handshake (DTR, RS423)
2	Input Handshake (TRXCA external clock)
3	Transmit Data-
4	Ground
5	Receive Data-
6	Transmit Data+
7	(Reserved)
8	Receive Data+

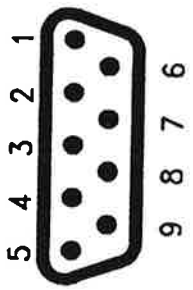


2.4.3 MFP SERIAL PORT PG. 3

The 68901 MFP also provides a slow speed RS232C serial port to the system. The baud rate clock for the MFP serial port transmitter and receiver is derived from the timer D output of the MFP. Given the MFP's 2.4576 MHz clock, baud rates up to 19.2Kbaud can be supported. The MFP serial port is connected to a DB-9P connector and contains a complete complement of modem control lines, (excluding Data Set Ready, pin 6).

2.4.3.1 MFP SERIAL PORT PINOUT

Pin	Function
1	Carrier Detect (In)
2	Receive Data (In)
3	Transmit Data (Out)
4	Data Terminal Ready (Out)
5	Ground
6	No Connect
7	Request to Send (Out)
8	Clear to Send (In)
9	Ring Indicator (In)

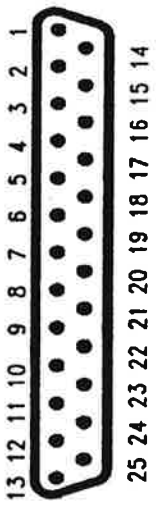


2.4.4 PARALLEL INTERFACE U305 PG. 3

The parallel interface is implemented through the programmable sound generator chip. It is a subset of the Centronics® standard and is output to a DB25 connector. The Centronics STROBE signal is generated from the PSG bit. The Centronics BUSY signal is connected to one of the parallel input lines of the MFP (U404) to permit interrupt driven printing. Eight bits of read/write data are handled through I/O port B on the PSG at a typical transfer rate exceeding 4 Kbytes per second.

2.4.4.1 PARALLEL PORT PINOUT

Pin	Function
1	STROBE
2	Data 0
3	Data 1
4	Data 2
5	Data 3
6	Data 4
7	Data 5
8	Data 6
9	Data 7
10	Not Connected
11	BUSY
12-17	Not Connected
18-25	Ground

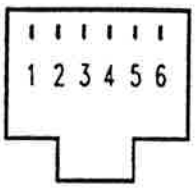


2.4.5 KEYBOARD INTERFACE

The keyboard transmits encoded make/break key scan codes (with two key rollover), mouse/trackball data, joystick data, and time-of-day. The keyboard receives commands and sends data via bidirectional communication implemented with an MC6850 Asynchronous Communications Interface Adapter (ACIA) and located in the keyboard. The data transfer rate is 7812.5 bits per second. The keyboard interfaces through a 6-pin telephone style jack.

2.4.5.1 KEYBOARD CONNECTOR PINOUT

Pin	Function
1	+5V
2	+5V
3	Transmit
4	Receive
5	Ground
6	Ground

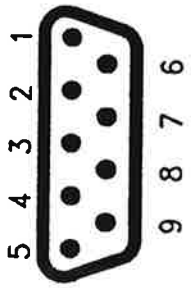


2.4.6 MOUSE AND JOYSTICK INTERFACE

The Atari two-button mouse is a mechanical, opto-mechanical, or optical mouse with the minimal performance characteristics of 100 counts/inch, maximum velocity of 10 inches per second, and maximum pulse phase error of 50 %. The joystick is a four direction switch-type joystick with one fire button. The mouse and joystick are connected via two DB-9P connectors located on either side of the keyboard. A mouse or joystick can be connected on the right side of the keyboard. The connector on the left side of the keyboard is for joystick only.

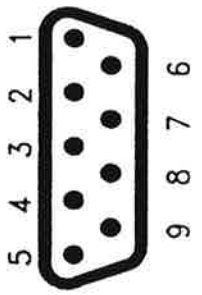
2.4.6.1 MOUSE/JOYSTICK CONNECTOR PINOUT

Pin	Function
1	Up XB
2	Down XA
3	Left YA
4	Right YB
5	Not Connected
6	Fire/Left Button
7	+5VDC
8	Ground
9	JOY1/Fire Right Button



2.4.6.2 JOYSTICK CONNECTOR PINOUT

Pin	Function
1	Up
2	Down
3	Left
4	Right
5	Reserved
6	Fire Button
7	+5VDC
8	Ground
9	Not Connected



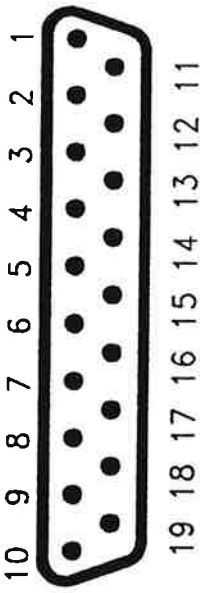
2.4.7 HARD DISK INTERFACE

Optional hard disks can be added to the system. The hard disk interfaces through the ACSI bus via a SCSI paddle board which plugs into the motherboard. The controller sends commands and data to the hard disk by way of the ACSI (Atari Computer System Interface) bus. All transfers to the hard disk are via DMA and the SCSI paddle board. DMA transfers are controlled by the SCSI paddle board via the HDRQ signal.

To access the SCSI paddle board the HDCS (Hard Disk Chip Select) signal is driven low and the CA1 signal to be asserted. The DMA support chip must respond with ACK low to acknowledge that data is on the bus or has been read from the bus. The Memory Controller internal to the GSTMCU then works with the DMA controller to write or read data from or into memory. Transfers can take place at up to 1 Mbyte per second.

2.4.7.1 EXTERNAL HARD DISK PINOUT (ACSI)

Pin	Function
1	Data 0
2	Data 1
3	Data 2
4	Data 3
5	Data 4
6	Data 5
7	Data 6
8	Data 7
9	Chip Select
10	Interrupt Request
11	Ground
12	Reset
13	Ground
14	Acknowledge
15	Ground
16	A1
17	Ground
18	Read/Write
19	Data Request



2.4.8 ROM CARTRIDGE

The MegaSTe® contains a ROM cartridge port that is fully compatible with the Atari ST® cartridges. The cartridge is physically connected through a 40-pin edge connector located on the left side of the case. ROM cartridges are mapped to a 128 Kbyte area starting at address FA0000 and extending to FB8FFF.

2.4.9 MUSICAL INSTRUMENT DIGITAL INTERFACE (MIDI)

The MegaSTe® is also equipped with a Musical Instrument Digital Interface (MIDI) which provides high speed serial communication of musical data to and from sophisticated synthesizer devices. The Musical Instrument Digital Interface (MIDI) allows the integration of the MegaSTe® with music synthesizers, sequencers, drum boxes, and other devices possessing MIDI interfaces. High speed (31.25 Kbaud) asynchronous current loop serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port).

MIDI specifies that data consist of eight data bits, one start bit, and one stop bit. The MIDI OUT and MIDI IN connector pinouts are as follows:

MIDI OUT

Pin	Function
1	THRU Transmit Data
2	Shield Ground
3	THRU Loop Return
4	OUT Transmit Data
5	OUT Loop Return

MIDI IN

Pin	Function
1	Not Connected
2	Not Connected
3	Not Connected
4	IN Receive Data
5	IN Loop Return

2.4.10 VME BUS PG. 9, 10

The VME bus is provided for system expansion. The bus is composed of 23 address lines and 16 data lines. Control for the bus is provided by PAL U903 (Pg. 9) and U904 (Pg. 9). External interrupt requests to the VME bus are handled by the SCU IC U801 (Pg. 8).

The VME bus in the MegaSTe® complies with the Vita C.1 specification. It supports A24/D16 or A16/D16 slave cards only.

2.5 SYSTEM STARTUP

After a RESET (power-up or reset button) the 68000 will start executing at the address pointed to by locations 4-7, which is ROM (GSTMCU maps the first 8 bytes of ROM at E00000-7 into addresses 0-7). Location 000004 points to the start of the operating system code in ROM. The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse to reset hardware registers).
2. Read the longword at cartridge address FA0000. If the data read is a "magic number", execute from the cartridge (ROM cartridge instructions take over here).
3. If not, continue.
4. Check for a warm start (see if RAM locations contain valid data), initialize the memory controller.
5. Initialize the PSG chip, deselect disk drives.
6. Initialize color palettes and set screen address.
7. If not a warm start, zero memory.
8. Set up operating system variables in RAM.
9. Set up exception vectors.
10. Initialize MFP.
11. Set screen resolution.
12. Attempt to boot floppy; attempt to boot hard disk; run program if succeeded.
13. If no boot disk, the 256K boot ROM will bring up the desktop.

2.6 SYSTEM ERRORS

The 68000 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen. The number of bombs equals the number of the exception which occurred.

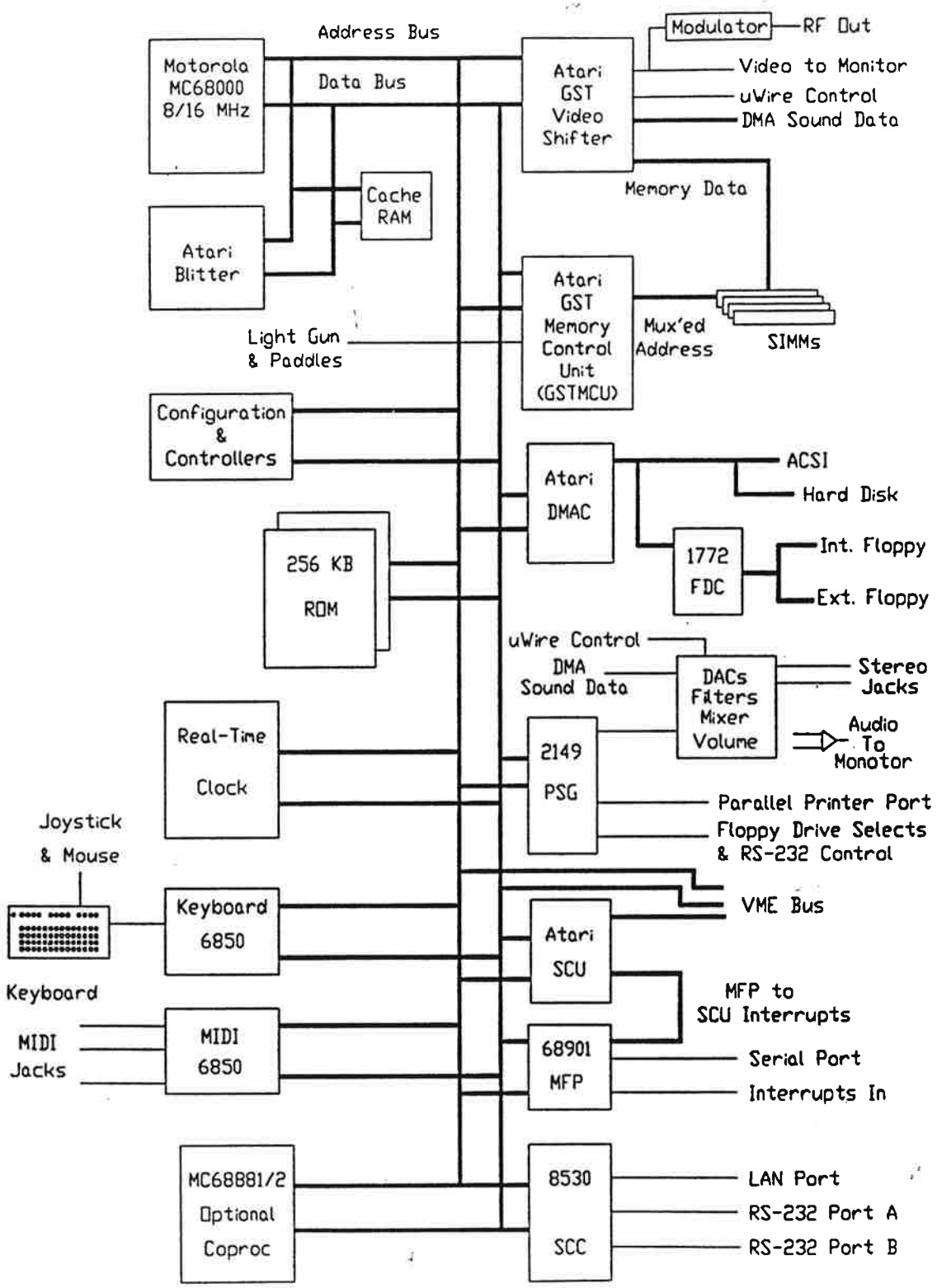
System errors may or may not be recoverable. Errors in loading files from disk may cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

2.6.1 NUMBER OF BOMBS AND MEANING

Bombs	Meaning
2	Bus Error. GSTMCU (U501) asserted bus error. This condition can be due to faulty MFP (U306), RAM (U701, U702, U703, U704), ROM (U206, U207), PSG (U305), or a short/open on the PCBA address/data lines.
3	Address Error. Processor attempted to access word or long word sized data on an odd address.
4	Illegal Instruction. Processor fetched an instruction from ROM or RAM which was not a legal instruction.
5	Zero Divide. Processor was asked to perform a division by zero.
6	Chk Instruction. This is a legal instruction, if software uses this, it must install a handler.
7	Trapv Instruction. See Chk instruction.
8	Privilege Violation. CPU was in user mode, tried to execute a supervisor instruction.
9	Trace. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.
10	Line 1010 Emulator. CPU read pattern 1010 as an instruction. Provided to allow user to emulate his own instructions.
11	Line 1111 Emulator. See Line 1010 Emulator.
12-23	Unassigned, should be no occurrence.
24	Spurious Interrupt. Bus error during interrupt processing.
25-31	Autovector Interrupt. Even numbered vectors are used, others should have no occurrence.

Bombs	Meaning
32-63	TRAP Instruction. CPU read instruction which forced exception processing.
64-79	MFP interrupts.
80-255	User interrupts.

2.7 ATARI MEGASTE BLOCK DIAGRAM



SECTION THREE

TESTING

3.1 OVERVIEW

This section pertains to the test equipment, diagnostic software, and test procedures used to verify correct operation and repair of the MegaSTe® computer. The diagnostic cartridge should be used if possible. If the unit gives no display or RS232 output when running the cartridge, see "Troubleshooting a Dead Unit" below.

Since the level of complexity in the MegaSTe® system is high, it should not be expected that this document can cover all possible problems or pinpoint the causes; rather, the intent here is to give a systematic approach which a technician can use to narrow down a problem to its most likely source. Experience in troubleshooting computer systems is assumed. Knowledge of the 68000 processor is helpful.

Economics will be an important consideration; due to the low cost of the MegaSTe® computer, little time can be justified in troubleshooting down to the component level when it may be cheaper to replace the functional subassembly. Many of the more expensive (and critical) components are socketed, making verification and replacement faster.

3.2 TEST EQUIPMENT

The following equipment will be needed to test the MegaSTe® computer:

- Atari SC1224 RGB Monitor
- Atari SM124 Monochrome Monitor
- SF314 External Floppy Disk Drive
- MegaSTe® Port Test Fixture
- RS232 Loop-Back Connector (3)
- MIDI Loop-Back Cable
- MegaSTe® Test Diagnostic Cartridge Rev. 1.3
- Blank Double Sided 3 1/2-inch Diskettes (2)
- LAN Loopback Connector

Optional (for troubleshooting):

- RS232 terminal (or STe® with VT52 emulator)
- RS232 Null Modem Cable

In addition, the following items may be required to troubleshoot and repair the unit:

- 2 Channel 100MHz Oscilloscope
- Small Hand Tools
- Spare Parts

3.3 TEST CONFIGURATION

With the power switch off, install the Diagnostic Cartridge with the label facing up.

IMPORTANT--if the cartridge does not have the plastic enclosure, BE SURE THE CARTRIDGE IS INSTALLED WITH THE CHIPS FACING DOWN).

Connect cables from the STe® test fixture into the hard disk port, parallel port, and joystick/mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the MIDI loopback cable and LAN loopback connector into their ports. Plug the color monitor into the monitor output (a monochrome can be used instead).

NOTE: THE RS232 LOOPBACK CONNECTORS SHOULD ONLY BE PLUGGED IN AFTER THE MENU IS DISPLAYED.

Make sure the switch on the STe® test fixture is in the position marked INT, otherwise the program will not proceed past the initialization. The other position is GENLOCK. The GENLOCK test is discussed later in section 3.4.4.

Power on the unit. Some tests will be run automatically; in a few seconds the menu screen should appear. If the screen appears, skip down to "MegaSTe® Diagnostic Cartridge", below. If not, read next section "Troubleshooting a Dead Unit".

3.4 TROUBLESHOOTING A DEAD UNIT

In the event that the system is correctly configured and powered on and no display appears, this is the procedure to use for determining the problem. This assumes elementary steps have been taken, such as checking the power LED to verify the unit is powered on and making sure the monitor is working. If the LED in the forward left corner is not illuminated, check the power supply voltages first. If voltages require adjusting, perform the adjustments. If the power supply is defective, replace the supply, then if the LED is still not illuminated, check to see if it is defective.

1. Connect a dumb terminal to the RS232 port of the unit under test (U.U.T.). You can use an STe® running the VT52 terminal emulator program. Please see the owner's manual for setting up VT52. The cable should connect pin 3 (serial out) of the U.U.T to pin 2 (serial in) of the terminal, and vice versa. Connect pin 7 (ground) to pin 7. The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity (this is the default condition for the VT52 emulator).
2. Insert the Diagnostic Cartridge into the U.U.T., and power on the unit. If the Diagnostic Cartridge messages appear on the display of the terminal, use the diagnostic to troubleshoot the computer. If not, the computer will have to be disassembled to troubleshoot. Refer to "MegaSTe® Diagnostic Cartridge" below for information on using the cartridge. If no activity is seen on the RS232 port or display, continue with (2) below.
3. Disassemble the computer so that the printed circuit board is exposed (see Section 4, Disassembly). Power up the computer. Using an oscilloscope, verify the 8 MHz clock to the 68000 CPU (pin 15). Replace oscillator if necessary. Then check pin 17 (HALT) of the 68000 CPU. It should be a TTL high. If so, go on to 5 below. If not, the CPU is halted. The reasons may be: (1) bad reset circuit, (2) double bus error, 3) bad CPU.
4. Check (1) by observing signal on input of the two inverters on the HALT line. Check (2) by observing pin 22 of the CPU (BERR) as the unit is powered on. It should be high always. If there are logic low pulses, some component is malfunctioning and GSTMCU is generating the error. Verify the clocks to GSTMCU and replace these components to verify them (if socketed).
5. If still failing, the CPU is unable to read ROM or there is a component which is not responding to a read or write by the CPU, probably the MFP 68901 or DMA Controller. The MFP should respond to an MFPCS with DTACK. The DMA chip should respond to FCS by asserting RDY. There is no way to check for a bad 68000 other than by elimination of the other two possibilities, although a hot CPU (too hot to touch for more than a second) strongly indicates a bad CPU.

6. If the CPU is not halted, it should be reading instructions from ROM cartridge, if installed, and data and address lines will be toggling. (If not, replace CPU.) At this point, there is the possibility that both the video and RS232 subsystems are failing. Verify the output of the MFP chip (pin 9) while powering on the unit with the cartridge installed. If data is being sent, trace it through the 1488 driver. Note that + and - 12v. is required for RS232. If all looks good, here may be something wrong with the connection to the terminal.

7. Verify also the output of the Video Shifter. If using an RGB monitor, check the outputs to the summing resistors for R, G, and B. Note that if BLANK is not going high, no picture will be possible. If using monochrome, check output pin 50. Also check the input to the MFP, pin 32, MONOMON-. Note that if the CPU does not read a low on this signal on power-up, it will cause RGB output on the Video Shifter.

8. If the Video Shifter is outputting a signal, but the picture is unreadable, there is probably a problem with screen RAM. The cartridge should be used to diagnose this problem, with the RS232 terminal as a display device.

3.4 MEGASTE® DIAGNOSTIC CARTRIDGE

The MegaSTe® Diagnostic Cartridge is used to detect and isolate component failures in the MegaSTe® computers. This document refers to revision 1.3. Users of earlier versions should refer to the appropriate Troubleshooting Guide. This section gives a brief guide to use with a description of each test, error codes or pass/fail criteria, and recommendations on repair.

3.4.1 POWER-UP

The diagnostic program performs several tests on power-up. In particular, the message "Testing MFP, GSTMCU timing, Video will appear, and the screen will appear scrambled for a few seconds before the menu is printed. The screen will turn red (dark background in monochrome) if an error occurs in the initial testing, with a message indicating the failure. The lowest 2 Kbytes of RAM is tested on power-up; if a location fails, the error will be printed to the RS232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there is no stack or system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen may turn red). Repair RAM.

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS232 port. The diagnostic program looks for keystrokes from the RS232 device.

If the display is unreadable, the RS232 terminal should be used. All messages are printed to the RS232 port as well as the screen.

3.4.2 POWER-UP INITIALIZATION ERRORS

INITIALIZATION (ERRORS OCCURRING BEFORE THE TITLE AND MENU APPEAR.)

I1 RAM data line is stuck.

I2 RAM disturbance. Location is altered by write to another location.

I3 RAM addressing. Wrong location is being addressed.

I4 MMU error. No DTACK after RAM access.

I5 RAM sizing error. Uppermost address fails.

I6 Bus Error handling failed. Bus Error occurred (on purpose), but caused a crash (e.g. system was unable to read the vector from RAM).

I7 Bus Error not detected. GSTMCU not asserting Bus Error or the signal is not reaching the 68000.

T0 MFP timers failed.

T1 Vertical sync timing failed.

T2 Horizontal sync timing failed.

T3 Display Enable Interrupt failed.

T4 Memory Controller video address counter failed.

T5 PSG Bus test. PSG chip is causing a bus error by staying on the data bus too long.

T6 Floppy Disk Controller Bus test. FDC chip is causing a bus error by staying on the data bus too long.

K0 Stuck key

K1 Keyboard controller is not responding.

K2 Keyboard controller reports error.

3.4.3 TEST MENU

The normal screen will be dark blue with white letters. The test title and revision number are displayed at the top, with the amount of RAM and keyboard controller revision below, and a test menu below that. To select tests, the user types the keys corresponding to those tests, and then the RETURN key. After the operator selects a test, the program will not proceed until the key break is detected (when the operator releases the key).

This prevents false "stuck key" messages in the keyboard test. Many iterations of the test or tests chosen can be run by typing in the number of cycles just before typing RETURN. Typing a zero will cause the test sequence to run continuously. To stop a cycle before completion, hit the ESC key (there may be some delay in some tests before the test stops). As each cycle completes, the total numbers of cycles will be displayed on the screen. Several hidden key sequences are also provided.

MAIN MENU:

Mega-STe® Field Service Diagnostic Test Rev. 1.3
© 1991, Atari Corp.
4M RAM Keyboard revision 2 60 Hz O.S. Version 2.02 USA NTSC

R RAM Test	O O.S. ROMs	K Keyboard
M MIDI	S Serial Port	T Timing
D DMA Port	I SCC	L Real-Time Clock
F Floppy Disk	P Printer/Mouse/Joy Ports	
G short BLiT	Y long BLiT	V VME

Q Run All Unattended Tests (R,O,K,M,S,T,D,I,L,F,P,Y,V)
Z Run Unattended Internal tests (R,O,K,G,T,V,L)

A Audio	C Color	H High resolution
J Hard Disk Read/Write		

E Examine/Modify memory
B Set RS232 rate
X Toggle video output--50/60 Hz
? Help

Enter Letter(s), and Return

HIDDEN KEY SEQUENCES:

<Shift> 1	System Clock 8 MHz cache off
<Shift> 2	System Clock 16 MHz cache off
<Shift> 3	System Clock 16 MHz cache on
<Shift> 5	8 MHz floppy clock set
<Shift> 6	16 MHz floppy clock set (1.44 Meg Drive)
<Shift> 7	Software Date

The RAM size, keyboard revision, O.S. version, country (or language), and television standard (PAL or NTSC) are shown.

The 'Q' selection sequences through all the tests except for Audio, Color, High resolution monitor, and Hard Disk Read/Write. The 'Z' selection sequences through RAM, ROM, Keyboard, short BLiT, Timing, VME, and Real-Time Clock. Selection 'E' enables the operator to examine or modify RAM or hardware registers. 'B' enables the operator to change the baud rate on the RS232 port. Pressing the up arrow increases it, pressing the down arrow decreases it.

For example T M2 L3 V0 <ENTER> would result in the Timing test being run once, MIDI test twicw, Real-Time Clock test three times, and VME indefinitely or until the <ESC> key is pressed.

After a test or series of tests completes, the pass/fail status and error report, if any, will be displayed. When the selected test(s) have passed the screen will turn green accompanied by a short beep. If the selected test(s) fails the screen will turn red accompanied by an audible tone which oscillates. This allows the user to perform other troubleshooting functions while the running diagnostics without having to look directly at the screen for an indication of a Pass or Fail status. Press the space bar to return to the menu.

If multiple tests are selected, the sequence can be halted before completion by pressing the ESC key. At the completion of the current test, the sequence will halt, with the options of either continuing or returning to the menu. In some cases there will be a considerable delay before the current test completes and the keystroke is detected.

3.4.4 SUMMARY OF TESTS

3.4.4.1 GENLOCK

The GENLOCK switch position allows the system to synchronize the MegaSTe® video with an external source. The system clock is also phase-locked to the input sync signal. To do this pin three of the monitor connector is grounded, and the external clock is sent to the system on pin 4.

The GENLOCK test can be run using the INT/GENLOCK switch on the MegaSTe® port test fixture. The GENLOCK test is run twice. Toggling the switch to the GENLOCK position on the STe® test fixture should switch between the normal menu and no menu. With no menu a "sweeping" cycle should be heard. Reset the computer between each change of the INT/GENLOCK switch.

NOTE: RUN THIS TEST ONLY WITH A COLOR MONITOR.

3.4.4.2 RAM TEST (R)

System RAM is tested in three stages: low 2 kbytes, middle (up to 64k), and from 64k to top. The test patterns used are: all ones, all zeros, a counting pattern (data=low word of the address), reverse counting pattern (data=complement of address low word). The counting pattern is copied from the top and bottom of a 32 Kbyte buffer into the current 32 Kbytes of video RAM, then shifts video RAM to a new area, verifies the pattern, and repeats the test, until the top of RAM is reached. Finally, addressing at 64k boundaries is checked by writing unique pattern in last 256 bytes of each 64k block. The cache RAM is also tested as well as a CAS1 test to detect opens and shorts on the CAS signal for the upper bank of memory.

If an error occurs, the display turns red accompanied by an oscillating tone and the error code is displayed, followed by the address, data written, data read, and the bits which did not agree.

For example: " R2 45603E W:603E R:613C bad bits: 1,8".

In units having more than one bank the address as well as the bit position must be used to find the correct SIMM. The following table gives a correspondence between the addresses and banks for various models:

ONE MEGABYTE MACHINES

Address	Bank	Bad Bit(s)	SIMM
0-07FFFF	bank 0	1-8	U703
	bank 0	9-16	U701
0080000-0FFFFF	bank 1	1-8	U704
	bank 1	9-16	U702

TWO AND FOUR MEGABYTE MACHINES

Address	Bank	Bad Bit(s)	SIMM
0-1FFFFF	bank 0	1-8	U703
	bank 0	9-16	U701
200000-3FFFFF	bank 1	1-8	U704
	bank 1	9-16	U702

A bank is 16 bits wide and consists of two 1Mbit X 8 SIMMS.

RAM ERROR CODES

Except where noted, repair by replacing the SIMM corresponding to the indicated bit(s).

R0	Error in low memory, possibly affecting program execution.
R1	Error in SIMM.
R2	Address error. Bad SIMM or memory controller. Address line not working.
R3	Address error at 64k boundary.
R4	Error during video RAM test. Bad SIMM.
Cache RAM	Error during cache RAM test. Bad cache RAM chip.

3.4.4.3 ROM TEST (O)

This test reads the configuration bytes of the operating system to determine the version, language/country, and TV standard (PAL or NTSC). All bytes from operating system ROMs are then read and the checksums are calculated and displayed. A CRC is then calculated for each EPROM.

The test fails if the CRC calculated does not match the CRC found in the last location in each EPROM (e.g. Version 2, French). Incorrect CRCs are indicated by the display turning red and an oscillating tone followed by a message. If an error is displayed, replace the corresponding ROM.

3.4.4.4 COLOR TEST (C)

This test verifies the Video Shifter. Seven color bands are displayed: red, green, blue, cyan, magenta, yellow, and white. Each band consists of 8 levels of intensity. All 16 color palettes are represented, each palette is a vertical strip across the screen (strips should not be discernable, but each color should be a straight line across the screen). Because of the tight timing involved, keystroke interrupts will cause the display to jitter.

The operator should see that there are no gaps or missing scan lines in the display. If lines are missing, check the three outputs on the Video Shifter for that color, and verify the values of the resistors on the output. Too low a brightness setting on the monitor will cause the monitor not to distinguish between fine levels, making it appear there are only four levels being output.

The Video Shifter has four outputs for red (R0,R1,R2,R3), green (G0,G1,G2,G3) and blue (B0,B1,B2,B3). Each of these outputs is summed together by a resistor network to give 8 levels of intensity for each color, depending on which of the outputs are on. The values of the resistors give different weight to each output. The value of the resistor at R0 is twice that of R1, which is twice that of R2. (Note: some versions have these resistors inside the shifter.)

This allows us to get 8 equal steps on the summed outputs. For example, R0 on and R1 and R2 off = 1/8, R0 off, R1 and R2 on = 7/8. This signal then passes through a transistor amplifier, and from there to the video monitor connector.

NOTE: THIS RESISTOR NETWORK IS INCORPORATED INTO THE GATE ARRAY CHIP IN LATER VERSIONS.

SYMPTOMS AND FIXES:

1. Missing primary color. Check the output of the transistor amplifier. Q503 is blue, Q502 is green, Q501 is red. Look for a staircase pattern (eight levels of intensity). If the signal is there, trace forward to the video connector, if not, trace backward to the Video Shifter, until the faulty component is found.
2. Primary colors present, secondaries missing or incorrect. Replace the Video Shifter (U502).
3. Coarse change in intensity (not a smooth dark to light transition). Replace Video Shifter (U502) or look for a short on the output of one of the three color outputs for the appropriate color.
4. Specks or lines on the screen. This can be caused by bad RAM; if RAM has been tested and is good, replace the Video Shifter (U502).
5. Wavering display, horizontal lines not occurring in the same place every time. The processor may be getting extra interrupts (if the processor is required to handle additional interrupts, it will not have time to change all color registers during a horizontal scan time). Examine the MFP interrupt request (pin 32). There should be an interrupt every 126 microseconds (2 display lines) from Display Enable (pin 20). If additional interrupts occur, locate the source: the inputs at pins 22-29 should all be high. If no external (to the MFP) source for the interrupts is found, replace the MFP (U306). NOTE: if the keyboard is not connected, the input to the 6850 will be low, causing continual interrupts.

3.4.4.5 KEYBOARD TEST (K)

Two types of test are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. The operator presses keys and observes that the corresponding character on the screen changes (reverses background color). The key will also be displayed in the lower half of the screen. The mouse buttons and four directions are also shown on the screen. Connect the mouse and move in any direction and the arrow will flicker. Any key clicks while the mouse is moving indicates a short.

NOTE: it is possible, if pressing keys very rapidly, to leave the representation of the key on screen in a depressed state. This does not indicate a problem with the hardware.

The self-test checks communication between the CPU and the keyboard microcomputer, and checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

KEYBOARD ERROR CODES

K0	Stuck key. A key closure was detected while the keyboard self test was executing.
K1	Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time. The keyboard needs to be replaced or the communication channel through the 6850 (U304) is not functional.
K2	Keyboard status error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status. Replace the keyboard.

3.4.4.6 MIDI TESTS (M)

This test sends data out the MIDI port, (data loops back through the cable) and reads from the input and verifies the data is correct. This also tests the interrupt from the 6850 through the MFP chip. The LED in the loopback cable will blink as data is sent (not all cables have the LED).

MIDI ERROR CODES

M0	Data not received. Trace the signal from the output of the 6850 (U303), through the drivers (U301), loopback cable, and receivers to the input of the 6850 (U303). Replace the defective component.
M1	Write/Read data mismatch. The data written was not the same as the data read. Replace 6850 (U303).
M2	Input frame error. Bad 6850 (U303) or bad driver (U301) or receiver causing noisy signal.
M3	Input parity error. Bad 6850 (U303) or bad driver (U301) or receiver causing noisy signal.
M4	Input data overrun. The 6850 received a byte before the previous byte was read. Probable bad 6850 (U303), also can be caused by the MFP (U306) not responding to the interrupt request.

3.4.4.7 SERIAL PORT TESTS (S)

NOTE: DO NOT INSTALL THE RS232 LOOPBACK CONNECTORS UNTIL AFTER THE MAIN MENU IS DISPLAYED.

First the RS232 control lines are tested (which are tied together by the loopback connector), then the data loopback is tested. Data is checked transmitting/receiving using a polling method first, then using interrupts.

Data is transmitted at 300, 600, 1200...19200 bps. Data transmission is performed by the MFP and the 1488 and 1489 driver and receiver chips (U310, U311). Interrupts are a function of the MFP (U306). Control lines are output by the PSG chip (U305) and input on the MFP. Note that this test does not thoroughly test the drive capability of the port. If the test passes, but the unit fails in use, it is likely that the 1488 (U311) or 1489 (U310) chips are bad.

SERIAL PORT ERROR CODES

Data transmission error:

S0	Data not received. Check signal path: MFP (U306) pin 9 to 1488 (U311) pin 5 to J305 pin 3 to J305 pin 2 to 1489 (U310) pin 1 to MFP (U306) pin 10.
S1	Data mismatch. Data read was not what was sent. Check integrity of the signal. May be bad driver (U311), receiver (U310), or MFP (U306).
S2	Input frame error. Incorrect time between start and stop bits. Probable MFP failure (U306).
S3	Input parity error. Input data had incorrect parity. Probable MFP failure (U306).
S4	Input data overrun. A byte was received before the CPU read the previous byte. MFP failure (U306) or, less likely, GSTMCU (U501) failure.
S5	No IRQ. CPU did not detect an interrupt by the MFP. MFP (U306) or GSTMCU (U501) failure.
S6	Transmit error. MFP (U306) transmitter failed.

SERIAL PORT ERROR CODES (CONTINUED)

S7	Transmit error interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.
S8	Receive error interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.
S9	RI/DTR connection. Signal sent at DTR is not detected at RI.
SA	DCD/DTR connection. Signal sent at DTR is not detected at DCD.
SB	RTS/CTS connection. Signal sent at RTS is not detected at CTS.
SC	RS232 input shorted to output. The input and outputs of the MFP serial port are shorted together.

3.4.4.8 SCC TEST (I)

The SCC diagnostic tests the SCC chip for several functions. Internal loopback polled (asynch), break (test ext loopback), external loopback polled (asynch), modem control lines, and external loopback interrupt (asynch). Ports A and B are tested in RS232 mode, and the LAN at port A is also tested.

SCC ERROR CODES

PORT A ERRORS:

SCC A internal loopback: Transmitter time-out	Transmitter failed.
SCC A internal loopback: Receiver time-out	Receiver failed.
SCC A internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC A internal loopback: Framing error	Incorrect time between start and stop bits.
SCC A internal loopback: Parity error	Input data had incorrect parity.
SCC A internal loopback: Data compare	Data read was not what was sent.

Port A has no loopback connector	The loopback connector is not installed on Port A.
LAN has no loopback connector	The loopback connector is not installed on the LAN Port.
LAN ERROR: DCD IS ACTIVE WITHOUT RTS ON	
	The Carrier detect signal is active without a request to send.
LAN ERROR: RTS IS ACTIVE BUT DCD IS NOT RESPONDING	
	The request to send signal is on but no carrier is active.
Port A async mode: Transmitter time-out	Transmitter failed.
Port A async mode: Receiver time-out	Receiver failed.
Port A async mode: Overrun	A byte was received before the CPU read the previous byte.
Port A async mode: Framing error	Incorrect time between start and stop bits.
Port A async mode: Parity error	Input data had incorrect parity.
Port A async mode: Data compare	Data read was not what was sent.
Port A modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port A modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port A modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

PORT B ERRORS:

SCC B internal loopback: Transmitter time-out	Transmitter failed.
SCC B internal loopback: Receiver time-out	Receiver failed.

SCC B internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC B internal loopback: Framing error	Incorrect time between start and stop bits.
SCC B internal loopback: Parity error	Input data had incorrect parity.
SCC B internal loopback: Data compare	Data read was not what was sent.
Port B has no loopback connector	The loopback connector is not installed on Port B.
Port B async mode: Transmitter time-out	Transmitter failed.
Port B async mode: Receiver time-out	Receiver failed.
Port B async mode: Overrun	A byte was received before the CPU read the previous byte.
Port B async mode: Framing error	Incorrect time between start and stop bits.
Port B async mode: Parity error	Input data had incorrect parity.
Port B async mode: Data compare	Data read was not what was sent.
Port B modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port B modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port B modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

SCC INTERRUPT ERRORS:

SCC interrupt error: Transmitter time-out	Transmitter failed.
SCC interrupt error: Receiver time-out	Receiver failed.
SCC interrupt error: Overrun	A byte was received before the CPU read the previous byte.

SCC interrupt error: Framing error	Incorrect time between start and stop bits.
SCC interrupt error: Parity error	Input data had incorrect parity.
SCC interrupt error: Data compare	Data read was not what was sent.
No Tx interrupt	A transmit command was issued but no interrupt occurred.
No Rx interrupt	A receive command was issued but no interrupt occurred.

3.4.4.9 AUDIO TEST (A)

This test requires the operator to decide subjectively if the test passes or fails.

PSG SOUND

A sound is output on each of the three sound generator channels. The 5/8 sound is a sweep from low to high frequency. Verify that the sound can be heard throughout the range with no drop in audio level.

DMA SOUND

Connect an oscilloscope at the stereo output jacks. Set the oscilloscope to 1 ms/division and 5 volts/division. There are four parts to this test. After observing the signals in each part of the test, proceed to the next part of the test by pressing the space bar. In each case the output signal amplitude should go from 0 volts to maximum amplitude in steps. The four parts of this test are as follows:

a. Mono 1 kHz. Both channels will output the same signal which should approximate a sine wave of 5-6 volts in amplitude.

b. Stereo 1 kHz/500 kHz. Verify that the right and left channels have the correct frequency. As one channel increases in amplitude, the other channel decreases. Maximum amplitude is 5-6 volts.

c. Treble. A 12.5 kHz signal is output on both channels. Maximum amplitude is about 6 volts.

d. Bass. a 50 kHz is output on both channels. Maximum amplitude is about 6 volts.

3.4.4.10 TIMING TESTS (T)

These tests are run at power-up as well as being selectable from the menu. The MFP timers, the GSTMCU timing for VSYNC and HSYNC, and video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as this test is run. There are two tests which check the bus timing for the Floppy Disk Controller and PSG chips. An error message is printed to the screen, then the test is run. If the test passes, the message is erased. If not, a Bus Error will occur and the message will remain. If a terminal is connected to the RS232 port, the message will not be erased, but "Pass" will be printed.

TIMING TEST ERROR CODES

T0	MFP timer error. One or more of the four timers in the MFP (U306) did not generate an interrupt on counting down .
T1	Vertical Sync. GSTMCU (U501) is not generating vertical sync in the required time period.
T2	Horizontal Sync. GSTMCU (U501) is not generating horizontal sync in the required time period.
T3	Display Enable. GSTMCU (U501) is not generating DE output or the MFP (U306) is not generating an interrupt.
T4	Video Counter in Memory Controller. The GSTMCU chip (U501) is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes.
T5	PSG Bus Test. The PSG chip (U305) is defective.
T6	1772 Bus Test. The Floppy Disk Controller chip (U405) is defective.

3.4.4.11 DMA TESTS (D)

Four sectors (2048 bytes) of data are written to the RAM on the port test fixture via high speed DMA, then read back and verified. This test is repeated many times for RAM addresses throughout the range of RAM.

DMA TEST ERROR CODES

D0	DMA time-out. No DMA occurred due to faulty DMA Controller (U404), GSTMCU (U501), or the HDINT interrupt was not processed by the MFP (U306). The failure can be isolated by seeing if the DMA Controller responds to HDRQ from the test fixture with ACK. Verify the MFP by seeing that the HDINT input causes an INTR output from the MFP.
D1	DMA count error. the number of bytes transferred was incorrect. The GSTMCU chip (U501) or DMA Controller (U404) is bad.
D2	Data data mismatch. The data received from the DMA port was not the same as the data sent. Replace the DMA Controller (U404). If the problem persists, check the data lines to the port for opens and shorts. A third possibility is that a defective Floppy Disk Controller (U405) is loading the bus.
D3	DMA not responding. Replace the DMA Controller (U404).

3.4.4.12 FLOPPY DISK TESTS (F)

In single test mode, a menu is displayed showing seven options:

1. Quick test. For each disk installed, formats, writes, and reads tracks 0, 1, and 79 of side 0. If double sided, formats and writes track 79 of side 1 and verifies that side 0 was not overwritten. If no disks are installed, checks to see what drives are on-line and if they are double or single sided. To assure that the drives are correctly tested, the operator should install (menu option 6) before calling the test. Once the test is run, the drives become installed, and will be displayed on the menu screen (below the RAM size).
2. Read Alignment Disk. Continuously reads a track, for checking alignment with an analog alignment diskette. The track to be read may be input by the operator. If "Return" is pressed without entering a number, the default is track 40.
3. Disk Interchange Test. Checks to see if diskettes from two disk drives each can be read by the other disk drive.
4. Disk Exerciser. A more thorough disk test; tests all sectors on the disk for an indefinite period of time.

5. Check copy protect tracks (80-82). Tests tracks 80-82, which are used by some software companies for copy protection. Not all manufacturers disk drives will write these tracks. NOTE: this test is for information only and should not be used to reject a mechanism.
6. Test Speed. The rotational speed of the drive is tested and displayed on the screen as the period of rotation. The acceptable range is 196-204 milliseconds. The highest and lowest values measured are displayed. The test stops when any key is pressed.
7. Install disk drives. Specify how many and what type of disks to test.

One additional test which can be performed is testing the write protect detection. Slide the write protect tab to the protected position, and run test #1. You should see "F5 Write protected" displayed if the drive has been installed, or "Unable to write disk" displayed if the drive has not been installed.

If more than one test is selected from the main menu, the floppy menu will not appear, but the Quick Test will be selected automatically.

FLOPPY TEST ERROR CODES

No floppies connected — The controller cannot read index pulses. The cable may be improperly connected, or the drive has no power, or the drive is faulty.

F0 — Drive not selected. Drive was installed, but failed attempting restore (seek to track 0). Check connection of cables, power to drive. Verify the light on the front of the drive goes on. Listen for the sound of the head seeking (the slide on the diskette should open). If all this occurs, TR0 (pin 23 on the Floppy Disk Controller U405) should go low. If so, check for an interrupt on pin 28 of the Floppy Disk Controller. If none, replace the Floppy Disk Controller (U405). Else trace the interrupt to the MFP (U306), verify that the MFP responds by asserting INTR. If the drive is not being selected (no light), check the PSG chip (U305). Pin 20 should go low when drive A is selected, and pin 19 should go low when drive B is selected. If not, replace the PSG (U305).

Error Writing (Formerly F1)

Error Reading (Formerly F2)

Error Formatting (Formerly F3)

Displays a more specific error message along with the above message such as F9 CRC error".

F4	Seek error. Verify that the STEP, MO, and DIRC outputs from the Floppy Disk Controller are sent to the drive. Probable failure in the Floppy Disk Controller (U405), but the drive is also suspect.
F5	Write protected. Check the write protect tab on the diskette. If OK, verify that the WP input (Floppy Disk Controller U405 pin 25) is going low during the test; if it is, then the Floppy Disk Controller is defective; if not, the problem is with the disk drive.
F6	Read compare error. Data read from the disk was not what was supposed to be written. Check in the following order: diskette, disk drive, Floppy Disk Controller (U405), and DMA Controller (U404).
F7	DMA error. DMA Controller could not respond to a request for DMA. Replace the DMA Controller (U404). If error persists, check FDRQ while running the test. It should normally be low and go high with each data byte transferred. If stuck high, push the reset button and verify that MR (Floppy Disk Controller U405 pin 13) goes low. If not, trace RESET to its source. If MR is OK, but FDRQ is still stuck, replace the Floppy Disk Controller (U405).
F8	DMA count error. Replace the GSTMCU (U501), if that does not fix it, replace the DMA Controller (U404).
F9	CRC error. The diskette or disk drive may be bad, else replace the Floppy Disk Controller (U405).
FA	Record not found. The Floppy Disk Controller could not read a sector header. May be a bad diskette, drive or Floppy Disk Controller (U405). If the test fails drive A but not drive B, the Floppy Disk Controller is not at fault (likewise fails B not A).

FB — Lost data. Data was transferred to the Floppy Disk Controller faster than the Floppy Disk Controller could transfer to the DMA Controller. If DMA Port test passes, the Floppy Disk Controller is probably bad (U405). The DMA Controller (U404) could also be at fault.

FC — Side select error - single sided drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.

FD — Drive not ready. The format/write/read operation timed-out. Probably a bad disk drive. Verify by checking another drive. Could also be a faulty Floppy Disk Controller (U405).

3.4.4.13 PRINTER AND JOYSTICK PORT TESTS (P)

The port test fixture is used to test the parallel printer port and joystick ports. The parallel port test writes to a latch on the test fixture and reads back data. The joystick port test outputs data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU. The cables connecting the joystick ports to the test fixture must not be reversed, or the printer and joystick tests will fail.

PRINTER/JOYSTICK ERROR CODES

P0 — Printer port error. Data read from the printer port was not what was written. Verify that the data lines on the PSG chip (U305 pins 6-13) are toggling when the test is run. If not, run the RS232 test. If the RI-DTR and DCD-DTR errors occur, the chip is probably not being selected. Check if the chip selects are being activated and the 2MHz clock is present. If the PSG is selected and not outputting signals, replace it (U305). If the data lines toggle, verify continuity. Also verify that J11 (Joystick 0) pin 3 is pulled up. Verify the test fixture is good by testing another computer. If it is OK, replace the PSG (U305).

P1 — Busy input error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected. If the P0 error also occurs, see handling for that. Otherwise, look for a signal arriving at MFP (U306) pin 25 from J304 pin 11. If no signal at J5, the test fixture may be bad. Verify with another computer.

J0	Joystick Port 0. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 12,10,9,8 respectively.
J1	Joystick Port 1. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 7,5,4,3 respectively.
J2	Joystick time-out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, keyboard-CPU communication line, or a faulty test fixture. If the power-up keyboard test passes, this eliminates any problem with keyboard-CPU communication.
J3	Left button input. If P1 error occurs, fix that first. Otherwise replace the keyboard.
J4	Right button input. If P1 error occurs, fix that first. Otherwise replace the keyboard.

3.4.4.14 HIGH RESOLUTION MONITOR (H)

If this test is selected while a color monitor is connected, a message is displayed to connect the monochrome monitor. The CPU waits for an interrupt from the MONOMON input to the MFP, and when received (the operator connects the monochrome monitor), changes the display to high resolution. The display screen shows horizontal and vertical lines, each 2 pixels in width. The screen will reverse every two seconds. When the operator sees the display is correct, he unplugs the monochrome monitor and re-connects the RGB monitor and the display should return to normal.

3.4.4.15 GRAPHICS CHIP (BLIT) (G,Y)

Two tests are available for this chip. The "short BLiT tests the ability of the blitter to move blocks of memory around and perform logical operations on the data. No patterns appear on the screen. If an error is detected, one of the error codes (G1-G12) is displayed.

In the "long BLiT test", a triangle is drawn on the screen and rotated 180 degrees until a rectangle is formed. If a color monitor is used, two identical images will be drawn. If an error occurs, the error code G14 will be displayed.

Corrective action for any error is the same: 1) verify the jumpers for the BLiT chip are installed correctly, 2) replace the chip (U205).

GRAPHICS CHIP ERROR CODES

G1	halftone RAM (internal RAM in BLiT chip)
G2	endmask
G3	operation
G4	halftone op
G5	skew
G6	reverse blt
G7	force extra source read
G8	smudge
G9	x count
G10	y count
G11	time-out
G12	address count
G13	Blitter Bus Error

3.4.4.16 REAL-TIME CLOCK (L)

The test saves the current time and date, and writes a new time, waits one second, and verifies that hours, minutes, seconds, etc. have all rolled over. This procedure is repeated for another date to verify all registers.

3.4.4.17 VME CONNECTOR (V)

This test is performed in two parts. The test is designed to check the bus connected to VME option cards, not the VME cards themselves. One part of the test requires that a XYCOM 4-port serial adapter be installed. The test is run and then the system is powered down and the board removed. The other part of the test requires that a Greenspring VME memory card be installed. The switches on the card must be set to 2 and 4 off and the rest on. The system is then powered up and the VME test run again. Failures during this test are most likely to show up as bad address or data errors.

3.4.4.18 HARD DISK READ/WRITE (J)

This tests the hard disk interface by writing and reading one complete track of the hard disk. It is not intended to test the hard disk drive. It does test the computer DMA circuitry. The test has been found to be more effective than the DMA test for some types of failures. These failures normally show up as "Data Compare" errors.

The test program will save the data on the cylinder used for testing and restore the data when the test is complete. (Quit or Park Heads is selected).

The test will run until the operator presses the ESC key. There is no pass condition. A failure will normally show up within a few seconds if it is going to occur.

HARD DISK READ/WRITE ERROR MESSAGES

Controller Not Responding.	This means there is no communication between the system and the hard disk. Cycling power on the hard disk may correct this condition.
Operation Timed Out.	The system sent a command which was accepted by the hard disk. The hard disk did not return a completion code in time.
Command Error.	The hard disk attempted to execute a command but an error in the hard disk occurred.
DMA Count Error.	After completing a data transfer the byte count of the data in system memory did not match the number of bytes sent.

Data Compare Error.	The data written to the hard disk and then read back did not match.

3.5 ERROR CODES QUICK REFERENCE

This is a brief summary of all error code which may occur when running the diagnostic.

INITIALIZATION (ERRORS OCCURRING BEFORE THE TITLE AND MENU APPEAR.)

I1	RAM data line is stuck.
I2	RAM disturbance. Location is altered by write to another location.
I3	RAM addressing. Wrong location is being addressed.
I4	MMU error. No DTACK after RAM access.
I5	RAM sizing error. Uppermost address fails.
I6	Bus Error handling failed. Bus Error occurred (on purpose), but caused a crash (e.g. system was unable to read the vector from RAM).
I7	Bus Error not detected. GSTMCU not asserting Bus Error or the signal is not reaching the 68000.

EXCEPTIONS (MAY OCCUR AT ANY TIME)

E1-E5	not used
E6	Autovector error. IPL0 is grounded or 68000 is bad.
E7	Spurious interrupt. Bus error during exception processing. Device interrupted, but did not provide interrupt vector.
E8	Internal Exception (generated by 68000).
E9	Bad Instruction Fetch.
EA	Address error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceded by a bus error or bad instruction fetch.

EB	Bus error. Generated internally by the 68000 or externally by GSTMCU. Usually caused by device not responding. Displays the address of the device being accessed.

RAM

R0	Error in low memory, possibly affecting program execution.
R1	Error in RAM chip.
R2	Address error. Bad RAM chip or memory controller. Address line not working.
R3	Address error at 64k boundary.
R4	Error during video RAM test. Bad RAM chip.
Cache RAM	Cache RAM failure.

KEYBOARD

K0	Stuck key
K1	Keyboard controller is not responding.
K2	Keyboard controller reports error.

MIDI

M0	Data not received.
M1	Data received is not what was sent.
M2	Data input framing error.
M3	Parity error.
M4	Data overrun. Byte was not read from the 6850 before next byte arrived.

RS232

S0	Data not received.
S1	Data received is not what was sent.
S2	Data input framing error.
S3	Parity error.
S4	Data overrun. Byte was not read from the MFP before the next byte arrived.
S5	IRQ. The MFP is not generating interrupts for transmit or receive.
S6	Transmitter error - MFP.
S7	No interrupt from transmit error (MFP).
S8	No interrupt from receive error (MFP).
S9	DTR - RI. These signals are connected by the loopback connector. Changing DTR does not cause change in RI.
SA	DTR - DCD. Same as S9 for these signals.
SB	RTS - CTS. Same as S9 for these signals.
SC	RS232 input shorted to output. The input and outputs of the MFP serial port are shorted together.

SCC ERROR CODES

PORT A ERRORS:

SCC A internal loopback: Transmitter time-out	Transmitter failed.
SCC A internal loopback: Receiver time-out	Receiver failed.
SCC A internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC A internal loopback: Framing error	Incorrect time between start and stop bits.

SCC A internal loopback: Parity error	Input data had incorrect parity.
SCC A internal loopback: Data compare	Data read was not what was sent.
Port A has no loopback connector	The loopback connector is not installed on Port A.
LAN has no loopback connector	The loopback connector is not installed on the LAN Port.

LAN ERROR: DCD IS ACTIVE WITHOUT RTS ON

The Carrier detect signal is active without a request to send.

LAN ERROR: RTS IS ACTIVE BUT DCD IS NOT RESPONDING

The request to send signal is on but no carrier is active.

Port A async mode: Transmitter time-out	Transmitter failed.
Port A async mode: Receiver time-out	Receiver failed.
Port A async mode: Overrun	A byte was received before the CPU read the previous byte.
Port A async mode: Framing error	Incorrect time between start and stop bits.
Port A async mode: Parity error	Input data had incorrect parity.
Port A async mode: Data compare	Data read was not what was sent.
Port A modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port A modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port A modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

PORT B ERRORS:

SCC B internal loopback: Transmitter time-out	Transmitter failed.

SCC B internal loopback: Receiver time-out	Receiver failed.
SCC B internal loopback: Overrun	A byte was received before the CPU read the previous byte.
SCC B internal loopback: Framing error	Incorrect time between start and stop bits.
SCC B internal loopback: Parity error	Input data had incorrect parity.
SCC B internal loopback: Data compare	Data read was not what was sent.
Port B has no loopback connector	The loopback connector is not installed on Port B.
Port B async mode: Transmitter time-out	Transmitter failed.
Port B async mode: Receiver time-out	Receiver failed.
Port B async mode: Overrun	A byte was received before the CPU read the previous byte.
Port B async mode: Framing error	Incorrect time between start and stop bits.
Port B async mode: Parity error	Input data had incorrect parity.
Port B async mode: Data compare	Data read was not what was sent.
Port B modem control error: DTR-DCD	Signal sent at DTR is not detected at DCD.
Port B modem control error: DTR-DSR	Signal sent at DTR is not detected at DSR.
Port B modem control error: RTS-CTS	Signal sent at RTS is not detected at CTS.

SCC INTERRUPT ERRORS:

SCC interrupt error: Transmitter time-out	Transmitter failed.
SCC interrupt error: Receiver time-out	Receiver failed.

SCC interrupt error: Overrun	A byte was received before the CPU read the previous byte.
SCC interrupt error: Framing error	Incorrect time between start and stop bits.
SCC interrupt error: Parity error	Input data had incorrect parity.
SCC interrupt error: Data compare	Data read was not what was sent.
No Tx interrupt	A transmit command was issued but no interrupt occurred.
No Rx interrupt	A receive command was issued but no interrupt occurred.

DMA

D0	Time-out. DMA did not take place, or interrupt not detected.
D1	DMA count error. Not all bytes arrived. Possible Memory Controller or GSTMCU error.
D3	DMA Controller not responding.

TIMING

T0	MFP timers failed.
T1	Vertical sync timing failed.
T2	Horizontal sync timing failed.
T3	Display Enable Interrupt failed.
T4	Memory Controller video address counter failed.
T5	PSG Bus test. PSG chip is causing a bus error by staying on the data bus too long.
T6	Floppy Disk Controller Bus test. Floppy Disk Controller chip is causing a bus error by staying on the data bus too long.

PRINTER AND JOYSTICK PORTS

P0	Printer port error.
P1	Busy (printer port input) failed.
J0	Joystick port 0 failed.
J1	Joystick port 1 failed.
J2	Joystick (keyboard controller) timed-out.
J3	Left button line failed.
J4	Right button line failed.

FLOPPY DISK DRIVE

F0	Drive off-line. Not responding to restore (seek track 0).

Former F1, F2, and F3 write and read errors are deleted. The message now will say "error writing" [or reading] and display the specific error found.)

F4	Seek error.
F5	Write protected.
F6	Data compare. (Data read not equal to data written.)
F7	DMA error.
F8	DMA count error (Memory Controller counter.)
F9	CRC error.
FA	Record not found.
FB	Lost data.
FC	Side select error.
FD	Drive not ready. Timed-out performing the command.

BLIT

G1	halftone RAM (internal RAM in BLiT chip)
G2	endmask
G3	operation
G4	halftone op
G5	skew
G6	reverse blt
G7	force extra source read
G8	smudge
G9	x count
G10	y count
G11	time-out
G12	address count
G13	Blitter Bus Error

REAL-TIME CLOCK

C0	no real-time clock
C1	increment error

SECTION FOUR

DISASSEMBLY/ASSEMBLY

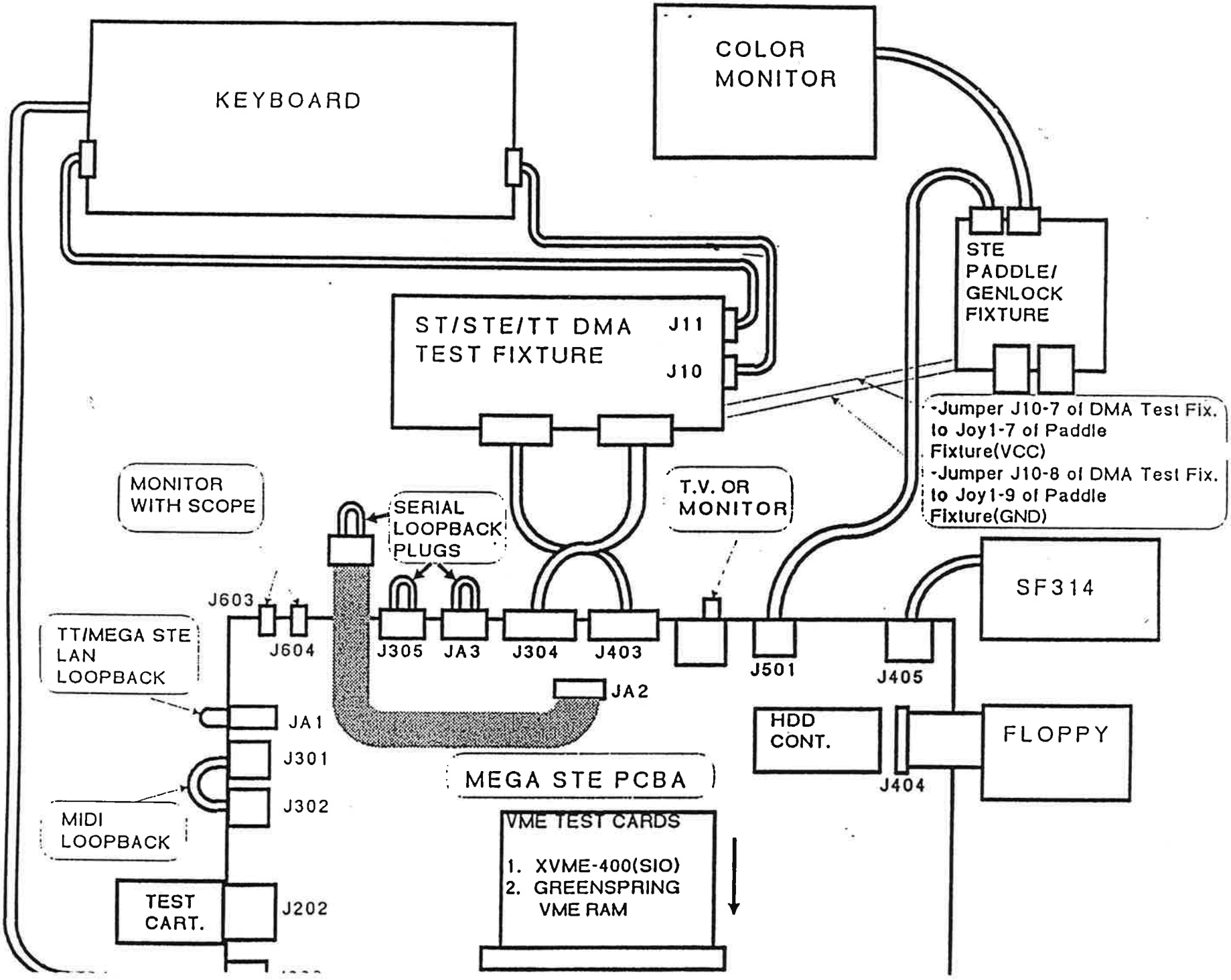
4.1 MEGASTE® DISASSEMBLY

Use the following procedure to disassemble the MegaSTe®.

Refer to Assembly Drawing, Section 7.

TOP COVER REMOVAL:

1. Turn off your computer and disconnect all cables from the sides and back of the unit (for example keyboard, power cord, external disk drive, and so on.).
2. Turn your computer over and place it on its top.
3. Remove the ten (10) screws located in the square holes on the bottom cover.
4. With a slotted screwdriver loosen the retaining screw holding the accessory cover in place.
5. While holding the computer's top cover and base together and holding the accessory cover in place turn the unit back over and set it on the bottom.
6. Lift up the front of the accessory cover and remove it from the computer. If a hard disk is present, set the hard disk on its side on the top cover. Disconnect the power and interface cables from the hard disk. Set the accessory cover aside.
7. Lift off the top cover and set it on its back behind the bottom case. Be sure to take care with the cables attached to the floppy disk drive and the power LED cable.
8. Disconnect the power, interface, and LED cables from the floppy drive.
9. Set the top cover aside.


KEYBOARD
COLOR MONITOR
STE PADDLE/ GENLOCK FIXTURE
ST/STE/TT DMA TEST FIXTURE
J11
J10
-Jumper J10-7 of DMA Test Fix. to Joy1-7 of Paddle Fixture(VCC)
-Jumper J10-8 of DMA Test Fix. to Joy1-9 of Paddle Fixture(GND)
MONITOR WITH SCOPE
SERIAL LOOPBACK PLUGS
T.V. OR MONITOR
SF314
J603
J604
J305
JA3
J304
J403
J501
J405
TT/MEGA STE LAN LOOPBACK
JA2
JA1
J301
J302
HDD CONT.
FLOPPY
J404
MEGA STE PCBA
MIDI LOOPBACK
VME TEST CARDS
1. XVME-400(SIO)
2. GREENSPRING VME RAM
TEST CART.
J202

FLOPPY DISK REMOVAL:

1. Remove the top cover.
2. Remove the 4 screws holding the floppy drive to the top cover.
3. Remove the 4 screws holding the floppy disk to the mounting plate.

HARD DISK REMOVAL:

1. Turn off your computer and disconnect all cables from the sides and back of the unit (for example keyboard, power cord, external disk drive, and so on.).
2. Turn your computer over and place it on its top.
3. With a slotted screwdriver loosen the retaining screw holding the accessory cover in place.
4. While holding the computer's top cover and base together and holding the accessory cover in place turn the unit back over and set it on the bottom.
5. Lift up the front of the accessory cover and set the hard disk on its side on the top cover. Disconnect the power and interface cables from the hard disk. Set the accessory cover aside.

POWER SUPPLY REMOVAL:

1. Remove the top cover.
2. Disconnect the power supply cables from the floppy disk drive and the hard disk drive if the hard disk is present.
3. Remove the two (2) screws holding the power supply in place and set them aside.
4. Remove the power supply and set it aside.

HARD DISK CONTROLLER BOARD REMOVAL:

1. Locate the hard disk controller board on the main PCB. Also locate the mounting screw attached to the standoff on the main PCB.
2. Disconnect the hard disk cable from the hard disk connector on the hard disk controller board.
3. Unfasten the hard disk controller board from the standoff on the main PCB using by removing the mounting screw.
4. Gently remove the hard disk controller board from the hard disk controller connector n the main PCB.

MAIN PCB REMOVAL:

1. Remove the top cover and set it aside.
2. Remove the three (3) screws from the main PCB and set them aside.
3. Remove the power supply and set it aside.
4. Remove the two (2) screws holding in any VME or serial connectors that are plugged into the VME slot and set them aside. Unplug the cable from the port serial board attached to the main printed circuit board.
5. Remove the board from the VME slot. Remove the reset button cap from the plunger on the reset switch.
6. Remove the main PCB.

4.2 MEGASTE® RE-ASSEMBLY

MAIN PCB:

1. Replace the main PCB.
2. Replace the board from the VME slot. Replace the reset button cap from the plunger on the reset switch.
3. Replace the two (2) screws holding in any VME or serial connectors that were plugged into the VME slot. Plug the cable from the serial board back into the main printed circuit board.
4. Replace the three (3) screws from the main PCB.

POWER SUPPLY:

1. Replace the power supply.
2. Replace the two (2) screws holding the power supply in place.
3. Reconnect the power supply cables from the floppy disk drive and the hard disk drive if the hard disk is present.

HARD DISK CONTROLLER BOARD

1. Install the hard disk controller board by lining up the hard disk controller connector on the main PCB with the main PCB connector on the hard disk controller board. The standoff and the standoff hole should also be lined up.
2. Gently push the hard disk controller board partially onto the hard disk controller connector on the main PCB. Make sure the connector pins of the main PCB connector are lined up with the socket connector on the hard disk controller board. Now push firmly down on the hard disk controller board until the connectors are fully engaged.
3. Fasten the hard disk controller board to the standoff on the main PCB using the mounting screw with the washer.
4. Reconnect the hard disk cable from the hard disk connector on the hard disk controller board.

FLOPPY DISK:

1. Replace the 4 screws holding the floppy disk to the mounting plate.
2. Replace the 4 screws holding the floppy drive to the top cover.

TOP COVER:

1. Set the top cover behind the base.
2. Reconnect the power, interface, and LED cables from the floppy drive.
3. Lift the top cover and set it back on the bottom case. Be sure to take care with the cables attached to the floppy disk drive, hard disk drive, and the power LED cable.
4. Install the back of the accessory cover to the accessory cover opening. Make sure the tabs on the back of the accessory cover line up with the slots in the accessory cover opening.
5. While holding the computer's top cover and base together and holding the accessory cover in place turn the unit over and set it on its top.
6. Replace the ten (10) screws located in the square holes on the bottom cover.
7. With a slotted screwdriver tighten the retaining screw holding the accessory cover in place.

HARD DISK:

1. Lift up the front of the accessory cover and set the hard disk on its side on the top cover. Disconnect the power and interface cables from the hard disk. Set the accessory cover aside.
2. While holding the computer's top cover and base together and holding the accessory cover in place turn the unit back over and set it on the bottom.
3. With a slotted screwdriver loosen the retaining screw holding the accessory cover in place.
4. Turn your computer over and place it on its top.

SECTION FIVE

SYMPTOM CHECKLIST

This section gives a brief summary of common problems and their most probable causes. For more detail, refer to the section on troubleshooting in this document, or the Diagnostic Cartridge Troubleshooting Guide.

DISPLAY PROBLEMS:

SYMPTOM	PROBABLE CAUSE
Black screen	No power (check power supply), bad GSTMCU chip (U501), bad Video Shifter (U502). See TESTING section, "Troubleshooting a Dead Unit".
White screen	Video Shifter (U502), GSTMCU (U501), DMA Controller (U404), 68000 (U007). Use diagnostic cartridge with terminal connected via RS232 port.
Dots/bars on screen	RAM, GSTMCU chip (U501), Video Shifter (U502). Use diagnostic cartridge.
One color missing	Check signals at video connector pins 3, 6, and 10. Check video cable, Video summer, buffer, Video Shifter (U502). Check signals with oscilloscope.
Monochrome Monitor Fails to Sync but Color Monitor Does	Verify monochrome monitor detect bit is not open when monochrome monitor is connected. Check connection at J501, check MFP (U306) pin 32, replace MFP.
Scrambled screen	GSTMCU chip (U501). Use diagnostic cartridge.

T.V. output bad	Modulator (U503), phase locked loop. Trace signal with oscilloscope.

DISK DRIVE PROBLEMS

SYMPTOM	PROBABLE CAUSE
Disk won't boot	Power supply, Floppy disk controller (U405), DMA Controller (U404), PSG chip (U305), disk drive. See if select light goes on, if not, check PSG outputs. Listen for motor spinning. If not, check power supply. Swap disk drive or try external drive. If not working, check DMA Controller (U404), Floppy disk controller (U405) with diagnostic cart.
Disk won't format	Floppy disk controller (U405), DMA Controller (U404), disk drive.
System crash after loading files	Diskette, disk drive, Floppy disk controller (U405), DMA (U404), or GSTMCU (U501). Swap diskette, retry. Use diagnostic cartridge to check Floppy disk controller, DMA Controller, GSTMCU, replace disk drive.

KEYBOARD PROBLEMS:

Bad keyboard, 6850 (U304), MFP (U306).

MIDI PROBLEMS:

Bad opto-isolator chip, 6850 (U303), inverter (U301).

RS232 PROBLEMS:

Bad MFP (U306), receiver (U310), driver (U311), or PSG chip (U305), power supply.

PRINTER PORT PROBLEMS :

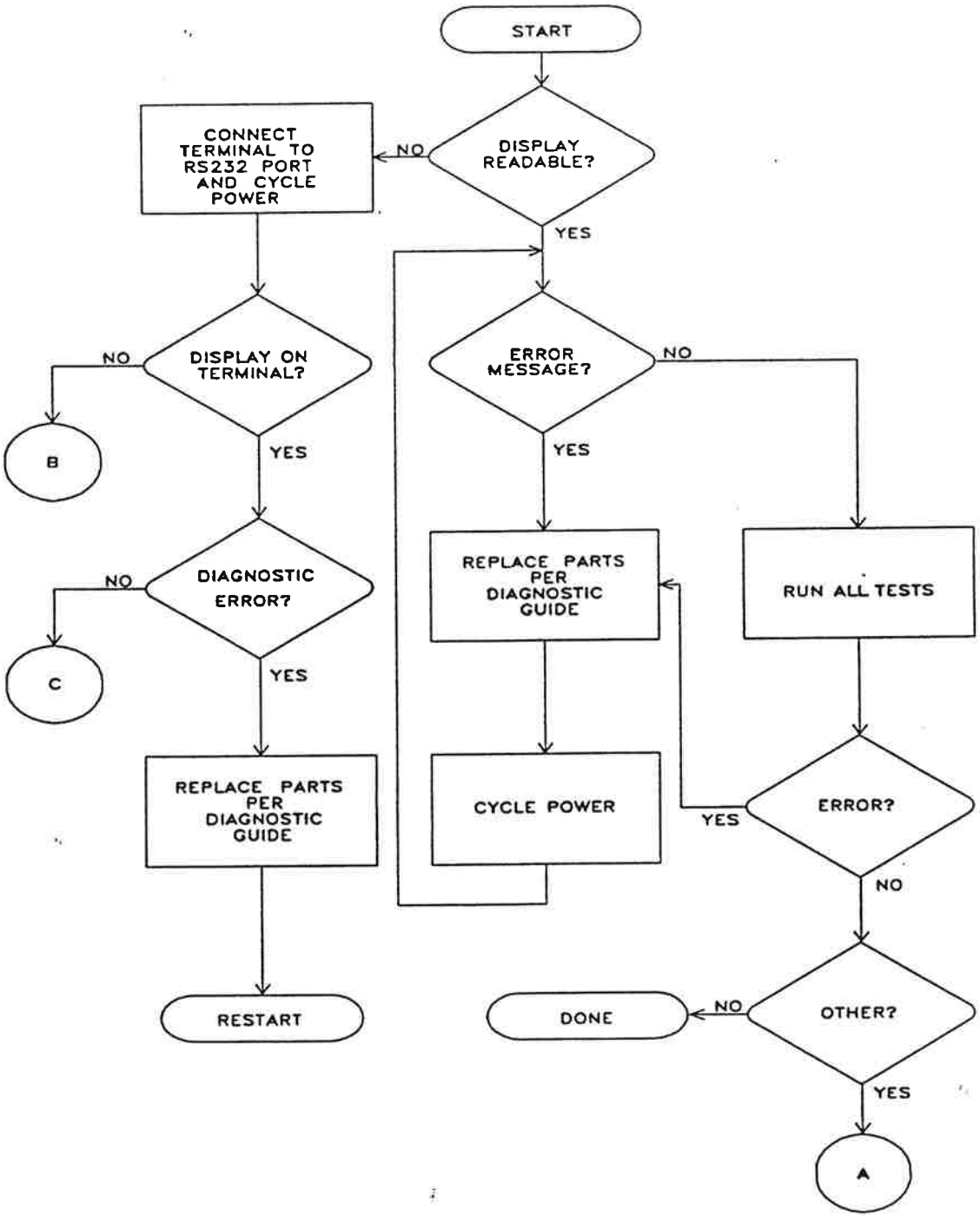
Bad PSG (U305), MFP (U306) chips.

HARD DISK PORT PROBLEMS:

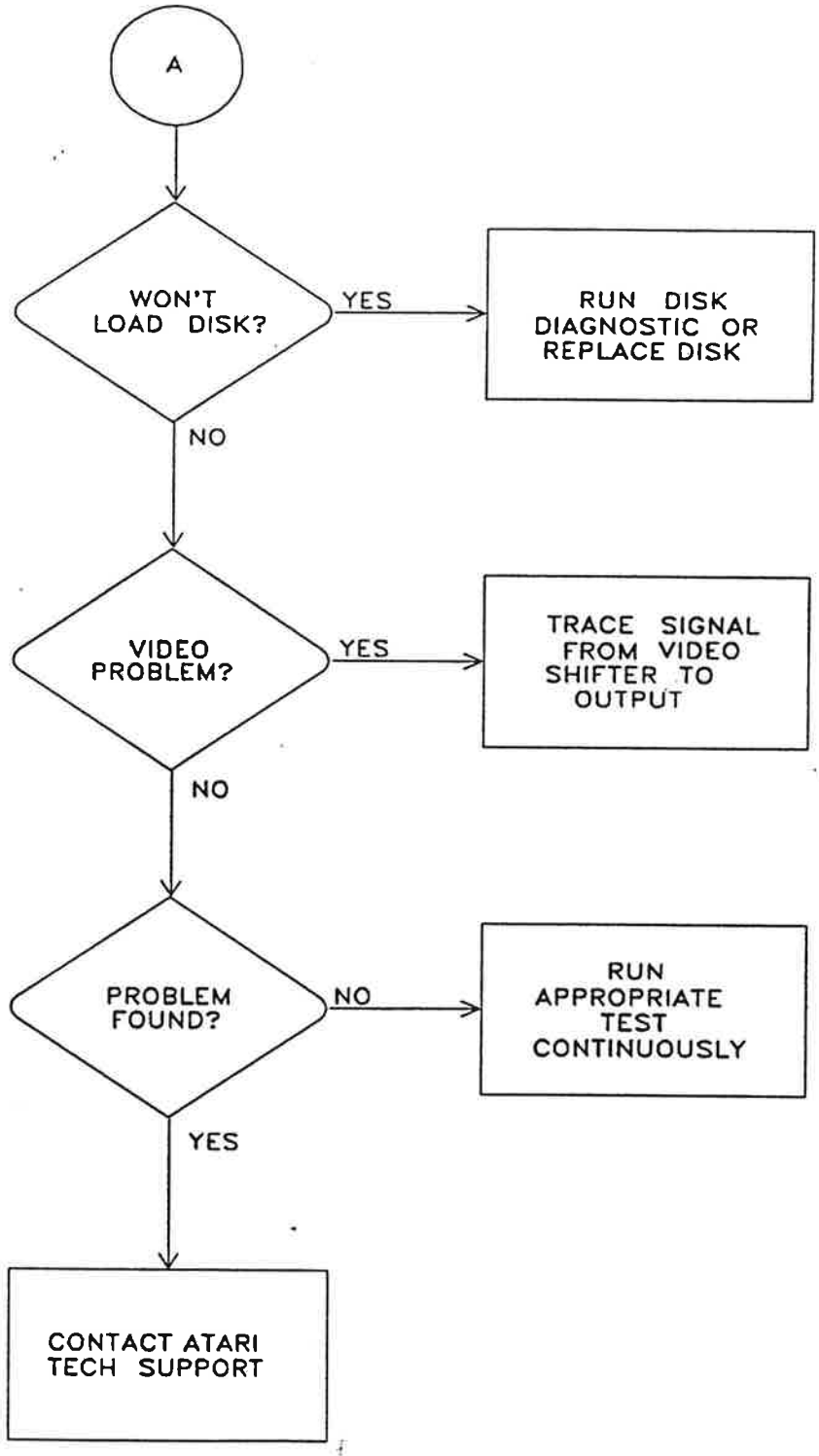
Bad DMA Controller (U404), GSTMCU (U501), Floppy disk controller (U405 loading the bus).

SECTION SIX

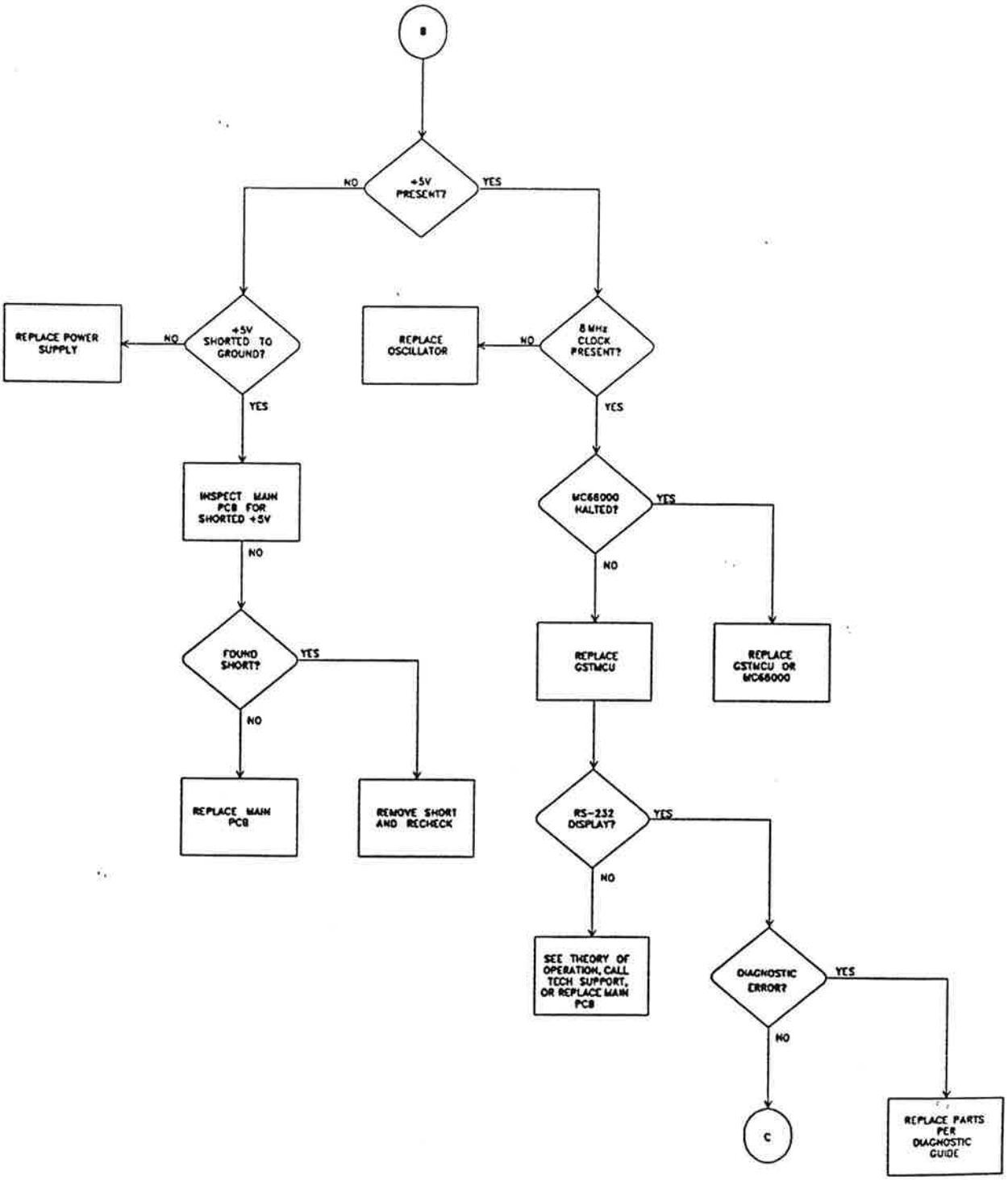
DIAGNOSTIC FLOWCHARTS



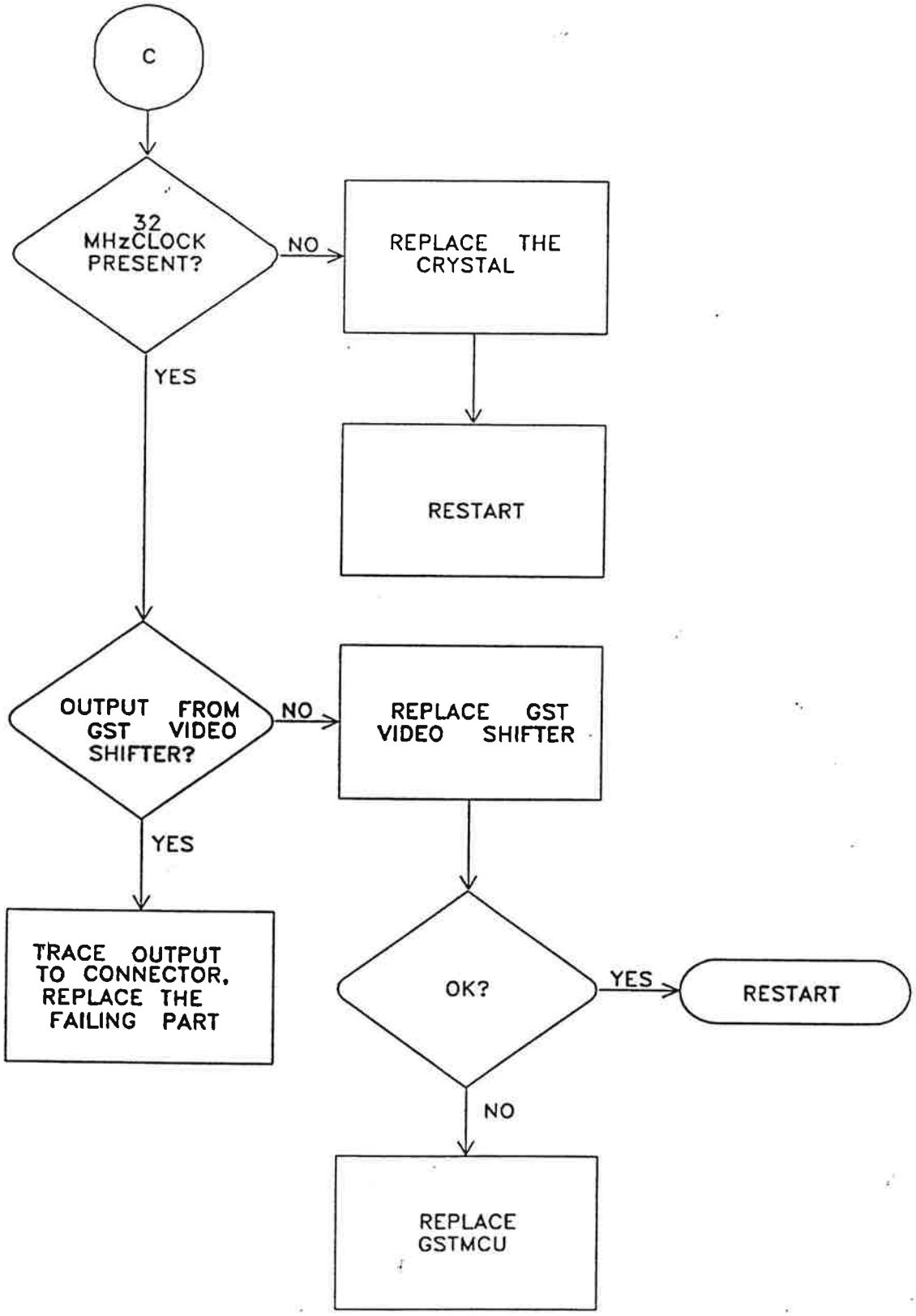
No Error on Diagnostic



No Display
No Monitor
No Terminal



NO DISPLAY OR ERROR



SECTION SEVEN

PARTS LIST AND ASSEMBLY DRAWINGS

MAJOR SUBASSEMBLIES

MAIN PCB ASSEMBLIES

1 MEGABYTE MEMORY--WITHOUT COPROCESSOR

ITEM	PART NUMBER	DESCRIPTION
9	CA400677-101	ASSY PCB MEGA STE/1 W/M USA
9	CA400677-102	ASSY PCB MEGA STE/1 W/M CAN
9	CA400677-103	ASSY PCB MEGA STE/1 W/M UK
9	CA400677-105	ASSY PCB MEGA STE/1 W/M GER
9	CA400677-106	ASSY PCB MEGA STE/1 W/M ITA
9	CA400677-107	ASSY PCB MEGA STE/1 W/H NET-UK
9	CA400677-108	ASSY PCB MEGA STE/1W/M NET-FRA
9	CA400677-109	ASSY PCB MEGA STE/1 W/H SPA
9	CA400677-110	ASSY PCB MEGA STE/1 W/M SWG
9	CA400677-111	ASSY PCB MEGA STE/1 W/M MEXICO
9	CA400677-112	ASSY PCB MEGA STE/1 W/M SWD
9	CA400677-114	ASSY PCB MEGA STE/1 W/M AUS
9	CA400677-120	ASSY PCB MEGA STE/1 W/M SWF
9	CA400677-104	ASSY PCB MEGA STE/1PERITEL FRA

1 MEGABYTE MEMORY--WITH COPROCESSOR

ITEM	PART NUMBER	DESCRIPTION
9	CA400677-001	ASSY PCB MEGA STE/1 W/M USA
9	CA400677-002	ASSY PCB MEGA STE/1 W/M CAN
9	CA400677-003	ASSY PCB MEGA STE/1 W/M UK
9	CA400677-005	ASSY PCB MEGA STE/1 W/M GER
9	CA400677-006	ASSY PCB MEGA STE/1 W/M ITA
9	CA400677-007	ASSY PCB MEGA STE/1 W/H NET-UK
9	CA400677-008	ASSY PCB MEGA STE/1W/M NET-FRA
9	CA400677-009	ASSY PCB MEGA STE/1 W/H SPA
9	CA400677-010	ASSY PCB MEGA STE/1 W/M SWG
9	CA400677-011	ASSY PCB MEGA STE/1 W/M MEXICO
9	CA400677-012	ASSY PCB MEGA STE/1 W/M SWD
9	CA400677-014	ASSY PCB MEGA STE/1 W/M AUS
9	CA400677-020	ASSY PCB MEGA STE/1 W/M SWF

2 MEGABYTES MEMORY--WITHOUT COPROCESSOR

ITEM	PART NUMBER	DESCRIPTION
9	CA400677-301	ASSY PCB MEGA STE/2 W/M USA
9	CA400677-302	ASSY PCB MEGA STE/2 W/M CAN
9	CA400677-303	ASSY PCB MEGA STE/2 W/M UK
9	CA400677-305	ASSY PCB MEGA STE/2 W/M GER
9	CA400677-306	ASSY PCB MEGA STE/2 W/M ITA
9	CA400677-307	ASSY PCB MEGA STE/2 W/M NET-UK
9	CA400677-308	ASSY PCB MEGA STE/2W/M NET-FRA
9	CA400677-309	ASSY PCB MEGA STE/2 W/M SPA
9	CA400677-310	ASSY PCB MEGA STE/2 W/M SWG
9	CA400677-311	ASSY PCB MEGA STE/2 W/M MEXICO
9	CA400677-312	ASSY PCB MEGA STE/2 W/M SWD
9	CA400677-314	ASSY PCB MEGA STE/2 W/M AUS
9	CA400677-320	ASSY PCB MEGA STE/2 W/M SWF
9	CA400677-304	ASSY PCB MEGA STE/2PERITEL FRA

2 MEGABYTES MEMORY--WITH COPROCESSOR

ITEM	PART NUMBER	DESCRIPTION
9	CA400677-201	ASSY PCB MEGA STE/2 W/M USA
9	CA400677-202	ASSY PCB MEGA STE/2 W/M CAN
9	CA400677-203	ASSY PCB MEGA STE/2 W/M UK
9	CA400677-205	ASSY PCB MEGA STE/2 W/M GER
9	CA400677-206	ASSY PCB MEGA STE/2 W/M ITA
9	CA400677-207	ASSY PCB MEGA STE/2 W/M NET-UK
9	CA400677-208	ASSY PCB MEGA STE/2W/M NET-FRA
9	CA400677-209	ASSY PCB MEGA STE/2 W/M SPA
9	CA400677-210	ASSY PCB MEGA STE/2 W/M SWG
9	CA400677-211	ASSY PCB MEGA STE/2 W/M MEXICO
9	CA400677-212	ASSY PCB MEGA STE/2 W/M SWD
9	CA400677-214	ASSY PCB MEGA STE/2 W/M AUS
9	CA400677-220	ASSY PCB MEGA STE/2 W/M SWF

4 MEGABYTE MEMORY--WITHOUT COPROCESSOR

ITEM	PART NUMBER	DESCRIPTION
9	CA400677-501	ASSY PCB MEGA STE/4 W/M USA
9	CA400677-502	ASSY PCB MEGA STE/4 W/M CAN
9	CA400677-503	ASSY PCB MEGA STE/4 W/M UK
9	CA400677-505	ASSY PCB MEGA STE/4 W/M GER
9	CA400677-506	ASSY PCB MEGA STE/4 W/M ITA
9	CA400677-507	ASSY PCB MEGA STE/4 W/M NET-UK
9	CA400677-508	ASSY PCB MEGA STE/4W/M NET-FRA
9	CA400677-509	ASSY PCB MEGA STE/4 W/M SPA
9	CA400677-510	ASSY PCB MEGA STE/4 W/M SWG
9	CA400677-511	ASSY PCB MEGA STE/4 W/M MEXICO
9	CA400677-512	ASSY PCB MEGA STE/4 W/M SWD
9	CA400677-514	ASSY PCB MEGA STE/4 W/M AUS
9	CA400677-520	ASSY PCB MEGA STE/4 W/M SWF
9	CA400677-504	ASSY PCB MEGA STE/4PERITEL FRA

4 MEGABYTE MEMORY--WITH COPROCESSOR

ITEM	PART NUMBER	DESCRIPTION
9	CA400677-401	ASSY PCB MEGA STE/4 W/M USA
9	CA400677-402	ASSY PCB MEGA STE/4 W/M CAN
9	CA400677-403	ASSY PCB MEGA STE/4 W/M UK
9	CA400677-405	ASSY PCB MEGA STE/4 W/M GER
9	CA400677-406	ASSY PCB MEGA STE/4 W/M ITA
9	CA400677-407	ASSY PCB MEGA STE/4 W/M NET-UK
9	CA400677-408	ASSY PCB MEGA STE/4W/M NET-FRA
9	CA400677-409	ASSY PCB MEGA STE/4 W/M SPA
9	CA400677-410	ASSY PCB MEGA STE/4 W/M SWG
9	CA400677-411	ASSY PCB MEGA STE/4 W/M MEXICO
9	CA400677-412	ASSY PCB MEGA STE/4 W/M SWD
9	CA400677-414	ASSY PCB MEGA STE/4 W/M AUS
9	CA400677-420	ASSY PCB MEGA STE/4 W/M SWF

CONTROLLER BOARDS

ITEM	PART NUMBER	DESCRIPTION
1	CA200535-001	HDD ASSY I/F LST-1/2/4

KEYBOARD/MOUSE ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
	CA400732-001	K/B MEGA STE USA
	CA400732-003	K/B MEGA STE UK
	CA400732-004	K/B MEGA STE FRA
	CA400732-005	K/B MEGA STE GER
	CA400732-006	K/B MEGA STE ITA
	CA400732-009	K/B MEGA STE SPA
	CA400732-010	K/B MEGA STE SWISS
	CA400732-012	K/B MEGA STE SWD
	CA070025	MOUSE ST/STE/MEGA

DISK DRIVES

ITEM	PART NUMBER	DESCRIPTION
	C103704-001	FDD 1MB 3.5" SONY W/LED

POWER SUPPLY

ITEM	PART NUMBER	DESCRIPTION
	C302074-001	PSU PHIHONG PSM 5341 FCC

MEMORY

ITEM	PART NUMBER	DESCRIPTION
8	CA400960-003	ASSY SIMM MODULE 512K X 8
8	CA400960-002	ASSY SIMM MODULE 1M X 8
8	CA400960-001	ASSY SIMM MODULE 1M X 8

ROM SETS

ITEM	PART NUMBER	DESCRIPTION
11	CA400857-001	ASSY IC TOS 2.05 USA
11	CA400857-003	ASSY IC TOS 2.05 UK
11	CA400857-004	ASSY IC TOS 2.05 FRA
11	CA400857-005	ASSY IC TOS 2.05 GER
11	CA400857-006	ASSY IC TOS 2.05 ITA
11	CA400857-009	ASSY IC TOS 2.05 SPA
11	CA400857-010	ASSY IC TOS 2.05 SWG
11	CA400857-012	ASSY IC TOS 2.05 SWD
11	CA400857-020	ASSY IC TOS 2.05 SWF

INTEGRATED CIRCUITS AND COMPONENTS

ITEM	PART NUMBER	DESCRIPTION
U004,U005	C302017-001IC	SRAM 8K X 8 85NS
U008,U009	C301846-001IC	CTRAM 8K X 8 35NS
U007	C398778-001IC	68000 PLCC 16 MHZ
U405	C026028-002IC	1772 FDD CONTROLLER
UB02	C101718-101IC	MC68881 16 MHz
U501	C301705-001IC	IMP GLUE CUSTOM TT
U502	C301712-001IC	SHIFTER
UA3	C301899-001IC	PAL 16R4
UA2	C301901-001IC	PAL 20L8
UB01	C301903-001IC	PAL 16L8
U6	C301904-001IC	GAL 22V10
U12	C301905-001IC	PAL 16L8
U3	C301906-001IC	GAL 22V10
U2	C301907-001IC	PAL 16R4B
U904	C301908-001IC	PAL 16L8A
U407	C301909-001IC	GAL 22V10
U306	C398106-001IC	MC68901 PLCC
UA04	C398109-001IC	Z85C30 10 MHz
U11	C301898-001IC	GAL 22V10
U404	C398739-001IC	DMA
U205	C101643	IC CUSTOM ST BLITTER
21	C301020-001	BATTERY 3.6V

SEPARATE ROMS

ITEM	PART NUMBER	DESCRIPTION
11	C302018-002IC	ROM MEGASTE TOS 2.05 E USA
11	C302019-002IC	ROM MEGASTE TOS 2.05 O USA
11	C302020-002IC	ROM MEGASTE TOS 2.05 E UK
11	C302021-002IC	ROM MEGASTE TOS 2.05 O UK
11	C302022-002IC	ROM MEGASTE TOS 2.05 E FRA
11	C302023-002IC	ROM MEGASTE TOS 2.05 O FRA
11	C302024-002IC	ROM MEGASTE TOS 2.05 E GER
11	C302025-002IC	ROM MEGASTE TOS 2.05 O GER
11	C302026-002IC	ROM MEGASTE TOS 2.05 E ITA
11	C302027-002IC	ROM MEGASTE TOS 2.05 O ITA
11	C302028-002IC	ROM MEGASTE TOS 2.05 E SPA
11	C302029-002IC	ROM MEGASTE TOS 2.05 O SPA
11	C302030-002IC	ROM MEGASTE TOS 2.05 E SWF
11	C302031-002IC	ROM MEGASTE TOS 2.05 O SWF
11	C302032-002IC	ROM MEGASTE TOS 2.05 E SWG
11	C302033-002IC	ROM MEGASTE TOS 2.05 O SWG
11	C302034-002IC	ROM MEGASTE TOS 2.05 E SWD
11	C302035-002IC	ROM MEGASTE TOS 2.05 O SWD

CABLE ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
3	CA400335-002	ASSY CABLE HDD MEGA STE
4	CA400336-002	ASSY CABLE FDD MEGA STE

LED ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
	CA400365-002	ASSY CABLE HDD/LED 180MM YELLOW
	CA400972-001	CABLE PWR ASSY 150MM DISK DRIVE
	CA400365-003	ASSY CABLE PWR/LED 550MM GREEN

MECHANICAL ASSEMBLIES

ITEM	PART NUMBER	DESCRIPTION
7	C300839-002	VME FILLER PANEL W/SERIAL HOLE
17	C301663-002	VME FILLER PNL MEGA STE
	CA400418-001	ASSY CABLE DB9(W/CONN SCREW)
24	C301562-001	BTM CASE MEGA STE
12	C300845-002	COVER HDD ACCESSORY MEGA STE
	CA400417-002	ASSY VME FILLER PANEL MEGA STE
10	CA400855-001	ASSY TOP CASE MEGA STE
	C300840-001	BRKT FLOPPY DRIVE
	C301894-001	BRKT RETAINER LED
	C300741-002	COVER HDD ACCESSORY MEGA STE
	C300835-001	SHIELD HARD DISK
	C300841-001	BRKT HARD DISK
	C070012	RUBBER FOOT

SECTION NINE

GLOSSARY OF PART NAMES AND TERMS

Bus Error	GSTMCU has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.
CPU	the 68000 microprocessor.
DMA	direct memory access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, takes place independent of the CPU, so the CPU can be processing while DMA is taking place. GSTMCU arbitrates the bus between the CPU and DMA.
DMA Controller	Atari proprietary chip which controls the DMA process. All disk I/O goes through this device.
Exception	a state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also Section Two, System Errors, or a 68000 reference for more detail.
Halt	state in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bi-directional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert HALT.

HSYNC	timing signal for the video display. Determines when the horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) also is encoded onto IPL1,2 as an interrupt to the CPU.
Interrupt	a request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities: the highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and GSTMCU.
GSTMCU	Atari proprietary chip which handles all RAM accesses. See Theory of Operation, Main System and Video Subsystem for details.
MIDI	Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the MegaSTe®, consists of a 6850 communications chip, driver and receiver chips (74LS04, 74LS05, and PC-900 photocoupler), and an MFP interrupt channel.
MFP	Multi-function Peripheral, also 68901. Interrupt control, timers, and USART for RS232 communication. See Theory of Operation, Main System.
Modulator	device which combines video signals R,G,B, VSYNC, and HSYNC into a composite signal for monitors requiring this type input, and also modulates this signal, combined with audio, onto an RF carrier for output to a television.
PLL	Phase Locked Loop ia a circuit which locks the horizontal sync signal onto the color burst reference frequency for accurate color on the T.V. Without this circuit, colors on the T.V. become unstable, flickering or shifting about on the screen.

PSG	Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.
RS232C	Electical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the ST® computers, consists of the MFP, PSG, 1488, and 1489 chips.
1772	Western Digital Floppy Disk Controller.
6850	also ACIA (Asynchronous Communication Interface Adapter). Interfaces between 8 bit parallel bus and serial communication bus. In the ST®, there are two 6850s, one for keyboard communication, and one for MIDI communication.
68901	see MFP.
Supervisor Mode	state of the CPU in which it is allowed to access all hardware and RAM locations, and perform some privileged instructions. Determined by the state of a bit in the Status Register. The operating system operates in supervisor mode, and switches to user mode before passing control to an application (although the application can enter supervisor mode if it wishes).
User Mode	state of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.
VSYNC	signal used for vertical synchronization of CRT display device. Occurs at 70 Hz (monochrome), or 50 or 60 Hz color.
YM2149	see PSG.

SECTION ONE
INTRODUCTION

The 520ST and 1040ST are designed as integrated units with keyboard, processor, memory, and I/O control in one package. The 520ST has 520 kbytes (524,280 exactly) of RAM, and the 1040ST has 1040 kbytes (1,048,568) of RAM. The 1040ST has a built in 1 Megabyte floppy disk drive, hence the full designation is 1040STF (floppy). Both 520ST and 1040ST are available with a modulator for T.V. output as an option. Models with a modulator are designated 520STM or 1040STFM. Early 520ST models have no modulator. Current models have circuitry for phase locked loop added on (April '86). Newer models will have the phase locked loop on the printed circuit board. The 1040ST (F, FM) has the power supply integrated into the package.

The main components are as follows:

520ST:

- Main board (with/without modulator)
- Keyboard assembly
- RF Shield (upper and lower)
- Plastic case (upper and lower)
- Mouse

1040ST:

- Main board (with/without modulator)
- Keyboard assembly
- RF Shield (upper, lower, and power supply)
- Power supply
- Disk drive
- Plastic case (upper and lower)
- Mouse
- Phase locked loop daughter board (units with modulator)

CASE DESIGN

The 520ST upper case has openings for the keyboard and a lens for the power indicator LED in the front left corner. (Fig. 1.1a).

The 1040ST case has in addition, a lens for the disk drive busy LED in the mid right side of the case (Fig. 1.1b).

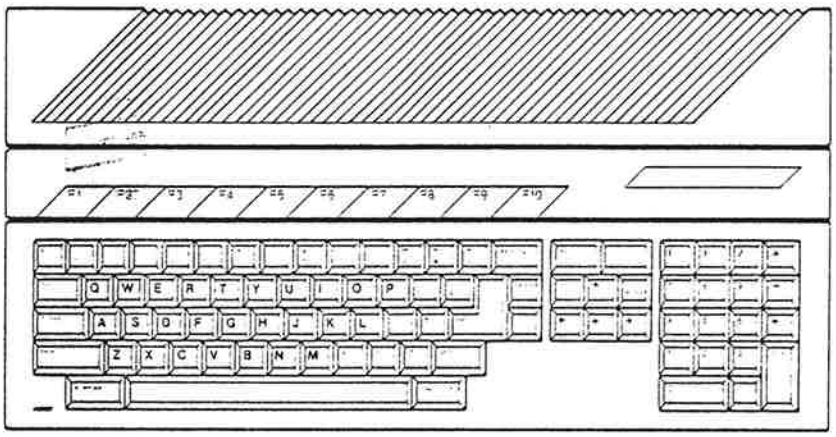


Figure 1.1a
520ST UPPER CASE

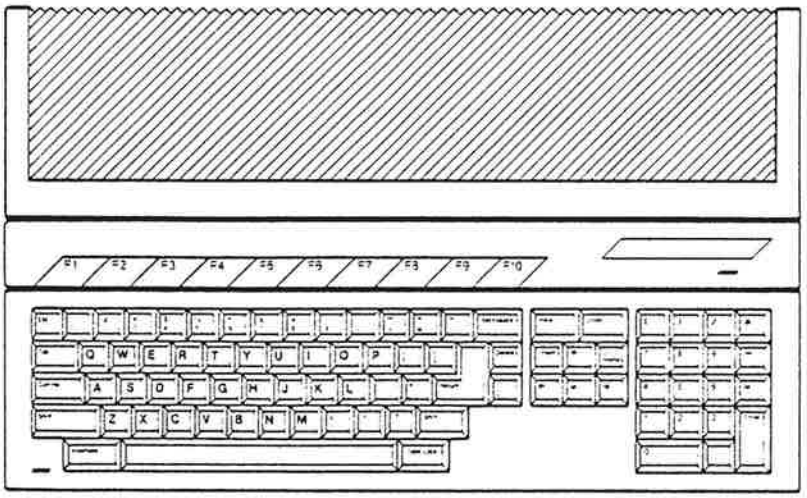


Figure 1.1b
1040ST UPPER CASE

The left side panel of the 520ST has a slot for the expansion cartridge (Fig. 1.2a).

The left side panel of the 1040ST has the cartridge slot and two ports for the MIDI connectors. (Fig. 1.2b).

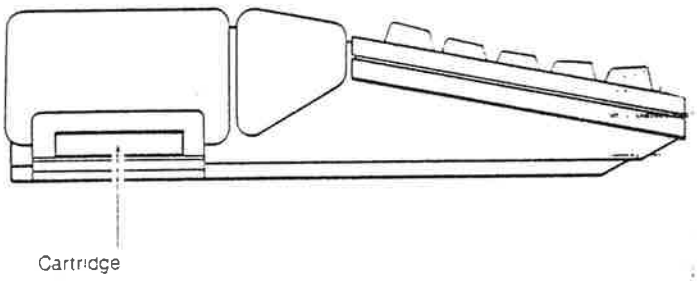


Figure 1.2a
520ST LEFT SIDE PANEL

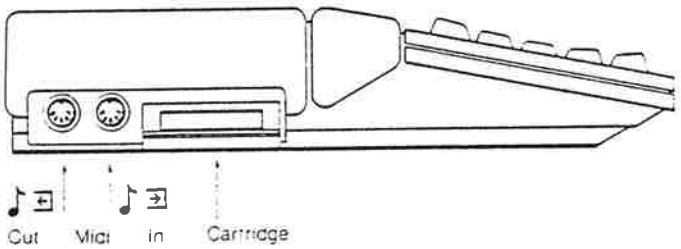


Figure 1.2b
1040ST LEFT SIDE PANEL

The right side panel of the 520ST has slots for the two joystick/mouse ports (Fig. 1.3a).

The right side panel of the 1040ST has a slot for the floppy disk drive. (Fig.1.3b).

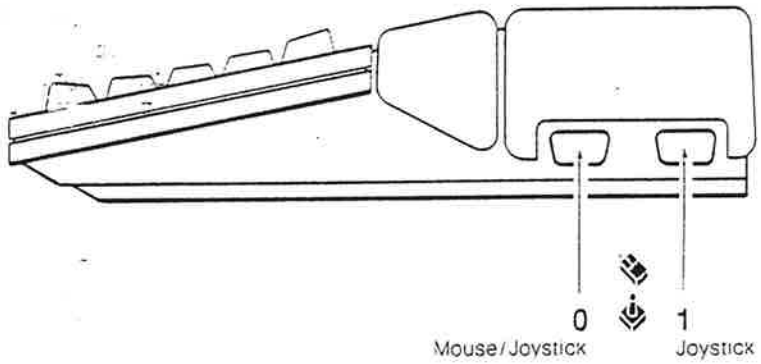


FIGURE 1.3a
520ST RIGHT SIDE PANEL

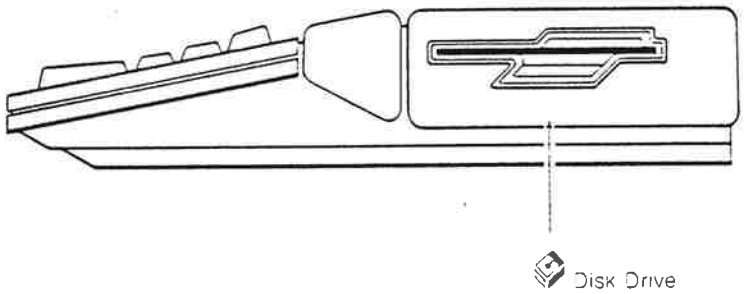


FIGURE 1.3b
1040ST RIGHT SIDE PANEL

The 520ST back panel contains (left to right) the reset button, power switch, D.C. power connector, MIDI ports, television output and channel select (optional), monitor connector, printer connector, RS232 (modem) connector, floppy disk connector, and hard disk connector (Fig. 1.4a).

The 1040ST back panel contains (left to right) the modem (RS232) connector, printer connector, hard disk connector, floppy disk connector, television output and select switch (optional), monitor connector, power switch, A.C. power input, and reset button. (Fig. 1.4b).

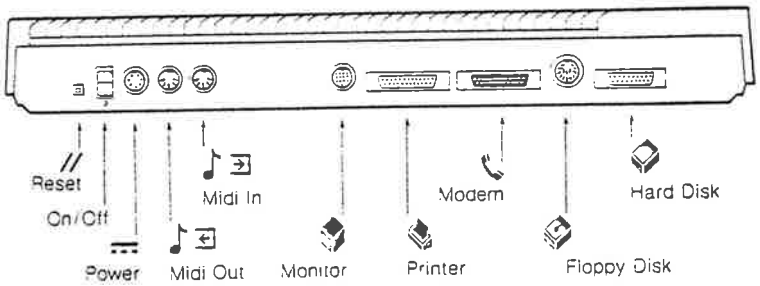


Figure 1.4a
520ST BACK PANEL

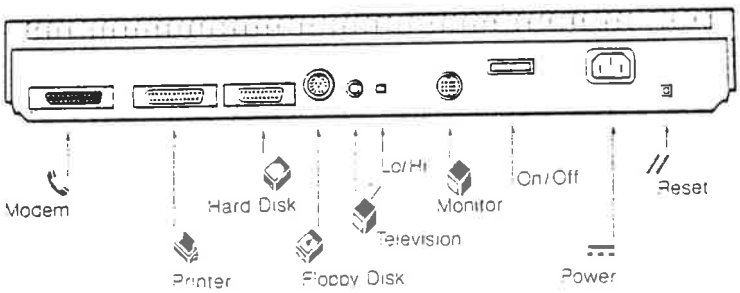


Figure 1.4b
1040ST BACK PANEL

POWER SUPPLY

The 520ST has a separate linear power supply providing regulated +5, +12, and -12 volts. There are no adjustments. The power supply can be disassembled by removing the four rubber pads on the underside, and removing the four screws from under the pads.

Power supply rating:
Current out: 3 A. at 5v., 30 mA. at +12v., 30 mA. at -12v.
Max. power in: 36 W.
Actual (in system) demand:
Typical current: 1.5 A. at 5v. 3 mA. at +- 12v. if RS232C is inactive. 19 mA at +12v., 18 mA at -12v. if RS232 is active.

The 1040ST has an integral switching power supply providing +5 and +12 volts. There is a 2 Amp. fuse and a voltage adjustment pot (single adjustment for both 5 and 12 volts). Voltage should be adjusted + or - 5% (4.75-5.25v). The power supply has over-current protection; if the fuse is blown, a catastrophic failure is likely, such as shorted primary.

Power supply rating:
Current out: 3 Amperes at 5v., .9 Amperes at +12v.
Max. power in: 33.5 W.
Actual (in system) demand:
Typical current: 2.2 A. at 5v., 160 mA. at +12v.
Max. current: 2.3 A at +5v., 340 mA. at +12 (during disk access).

SECTION TWO
THEORY OF OPERATION

OVERVIEW

The 520ST and 1040 ST share a common architecture, using the same LSI chip set. The most significant difference is the addition of one bank of 512K of RAM, for a total of 1024K (1,048,568 bytes). Except for the additional RAM, the differences between the 520 and 1040 are transparent to software. The hardware can be considered as consisting of a main system (central processing unit and support chips) and several Input/Output subsystems.

Main System

* MC68000 running at 8MHz
* 192 Kbyte Read Only Memory (64k in early versions)
* 1024 Kbyte Random Access Memory
* Direct Memory Access support
* System timing and Bus control
* Interrupt control

Audio/Video Subsystem

* BitMapped video display, using 32k bytes of RAM, relocatable anywhere in memory. There are three display modes available:
    1. 320 x 200 pixel, 16 color palette from 512 selections
    2. 640 x 200 pixel, 4 color palette from 512 selections
    3. 640 x 400 pixel, monochrome
* Monitor interface: RGB, Monochrome, Composite (STM and STFM only)
* Audio output: programmable sound chip
* Television interface (STM and STFM only)

Input/Output Subsystems

* Intelligent Keyboard with 2 button mouse/joystick interface
* Parallel printer interface
* RS-232C serial interface
* Floppy disk drive & connector for external drive
* Hard disk drive interface
* Musical instrument network communication: Musical Instrument Digital Interface (MIDI).

MAIN SYSTEM

The main system includes the microprocessing unit, main memory (ROM and RAM), system control, interrupt control, and general purpose DMA controller.

Microprocessing Unit

The ST's use the Motorola MC68000 16 bit external/32 bit internal data bus, 24 bit address bus microprocessor, running at 8 MHz.

Glue

Glue (named because it holds the system together) is such an important component that it is involved in nearly every operation in the computer. The functions may be summarized as follows:

Clock dividers— takes the 8 MHz clock and outputs 2 MHz and 500 KHz clocks.

Video timing— Blank, DE (Display Enable), Vsync, and Hsync are used to generate signals for the video display. There is a Read/Write register in Glue which may be written to configure for 50 or 60 Hz operation (done by the Operating System).

Interrupt priority— interrupts from the MFP and video timing are coded into four levels of priority on outputs IPL1 and IPL2 to the 68000. These levels correspond to no interrupts, MFP interrupts, VSYNC interrupt, HSYNC interrupt.

Signal and Bus arbitration— Glue decodes addresses to generate chip selects to the 6850s, MFP, DMA Controller, Programmable Sound Generator, Memory Controller, and ROMs. It receives signals from the MFP, DMA, Memory Controller, to synchronize data transfer. It arbitrates the bus during DMA transfers to prevent CPU and DMA devices from interfering with each other (see DMA below).

Illegal condition detection—Glue asserts Bus Error (BERR) if certain conditions are violated, such as writing to ROM, writing byte sized data to a word sized register, or writing to system memory when the processor is in user mode. Also occurs if a device does not respond within the required time limit. For example, the CPU tries to read from memory and the Memory Controller does not assert DTACK.

Main Memory

Main memory consists of 192 kbytes of ROM and one or two banks (512 Kbyte each) of dynamic RAM. In addition, the cartridge slot allows access to 128 Kbytes of ROM. All memory is directly addressable. The components of the memory system are: ROM, RAM, RAM buffers, Memory Controller, and Glue. The Operating System resides mostly in ROM, with optional segments loaded from disk into RAM.

RAM is organized as 16 bit words and may be accessed 16 bits at a time or 8 bits at a time. Even numbered addresses refer to the high 8 bits of a word and odd addresses refer to the low 8 bits. RAM is made up of 256 kbit X 1 chips; in the 520ST there are 16 chips, giving 512 kbytes, while in the 1040ST there is an additional bank of 16 chips, giving two times the memory, or Mbyte.

RAM memory map:

000008-000800	System memory (priveliged access)
000800-07FFFF	low bank
080000-0FFFFF	high bank (1040 only)

Note: the first 8 bytes of ROM are mapped into addresses These are reset vectors which the 68000 uses on start-up.

The Operating System is located in six 32k x 8 ROM chips in current versions (192k). Some early versions of the 520ST have only two 8k x 8 boot ROMs (16K), and load the operating system from disk into RAM. Even if the O.S. is in ROM, if a boot disk is in the floppy at power-on, the O.S. will load into RAM and take control.

ROM memory map:

high,low	192k	16k
U4,U7	FC0000-FCFFFF	FC0000-FC4000
U3,U6	FD0000-FDFFFF	
U2,U5	FE0000-FEFFFF	

Memory Controller--takes addresses from the address bus and converts to Row Address Strobe (RAS) and Column Address Strobe (CAS). All RAM accesses are controlled by this Atari proprietary chip, which is programmable for up to 4 Megabytes of memory. The Operating System determines how much memory is present and programs the Memory Controller at power-up. The Memory Controller refreshes the dynamic RAMs, loads the Video Shifter with display data, and gives or receives data during direct memory access (DMA).

Glue--decodes addresses for RAM and ROM and asserts output signals to enable these devices (also decodes addresses for most hardware registers to provide chip selects, as well as many other functions. See Glue description above.).

Direct Memory Access

Direct memory access is provided to support both low speed (250 to 500 Kilobits/sec) and high speed (up to 8 Megabits/sec) 8 bit device controllers. The floppy disks transfer data via low speed DMA and the hard disk (or other devices on the hard disk port) transfer at high speed. For DMA to take place, the Memory Controller is given the address of where to take data from or put data in RAM, the DMA Controller is set up (which channel, high speed or low speed, and how many bytes) and the peripheral is given a command to send or receive data. The entire block of data (the size must be given to the DMA Controller and the peripheral before the operation starts) is then transferred to or from memory without intervention by the CPU.

For example, in a transfer of a sector from the floppy to memory, the floppy controller will signal the DMA Controller that a byte is ready by asserting FDRQ, the DMA chip will read the byte and signal Glue, Glue will signal the Memory Controller, and the Memory Controller will read the byte from the DMA Controller and place it in the address which was set up previously. The DMA Controller will then wait for the next byte from the floppy controller, and the process will repeat until the specified number of bytes has been transferred. Transfers from memory to floppy are similar. The floppy initiates every transfer by requesting data on FDRQ.

At high speed (hard disk port), there is a difference: as a byte is ready to transfer to or from the DMA chip, the DMA Controller will assert ACK to let the peripheral know the byte is available or has been read. The DMA Controller can store up to 32 bytes in internal memory. This is necessary if the 68000 is using the bus, and the DMA must wait to transfer to memory. Data may be input from the port without being lost or slowing down the transfer speed.

MFP Interrupt Control

The 68901 MFP handles up to 16 interrupts. Currently all but one are used. Each interrupt can be masked off or disabled by programming the MFP. The 8 inputs are also directly readable by the CPU. When the MFP receives an interrupt input, or generates an interrupt internally, if the interrupt is enabled, MFPINT will be driven low. When the CPU is ready to respond, it signals interrupt acknowledge (FC0-2 high and VMA low) and Glue will assert IACK (interrupt acknowledge). The MFP will assert DTACK and put a vector number on the data bus, which the CPU will read and use to calculate the address of the interrupt routine.

The interrupts controlled by the MFP are: monochrome monitor detect (MONOMON), RS232 (including CTS, DCD, RI), disk (FDINT and HDINT), parallel port BUSY, display enable (DE, equals start of display line), 6850 IRQs for keyboard and MIDI data, and MFP timers.

Not all I/O operations use interrupts. The CPU can also poll the MFP while waiting for an operation to complete.

The MFP has four timers, used by the Operating System for event timing and used by the RS232 port for transmit and receive clocks.

AUDIO/VIDEO SUBSYSTEM

The video subsystem consists of the video display memory, the Memory Controller, Glue, a graphics control chip (Video Shifter), some discrete components to drive the video output, and an RF modulator (STFM version). The audio subsystem consists of a Programmable Sound Generator chip with a transistor output amplifier.

Video Shifter

There are 16 color palette registers in the shifter. All 16 are may be used in low resolution, 4 may be used in high resolution, and only one is used in high resolution (actually, only bit 0 of register 0 is used for inverse/normal video). Each palette is programmed for 8 levels of intensity of red, blue, and green, so there are 8 x 8 x 8 = 512 colors possible. For a given pixel, the color which is displayed is taken from the palette referred to by getting information from each logical plane (see description of video display memory below). The shifter will output the red, green, and blue levels specified by that palette; note there are three outputs for each color. Each output is either on or off. Thus, the number of possible output levels is 2 to the 3rd power = 8. The three outputs are summed through a resistor network to proportion the voltage level to give 8 equal steps. In monochrome mode, the color palettes are bypassed and there is a separate output.

Video Display Memory

Display memory is part of main memory with the physical screen origin located at the top left corner of the screen. Display memory is configured as 1, 2, or 4 (high, medium, or low resolution) logical planes interwoven by 16 bit words into contiguous memory to form one 32 Kilobyte physical plane starting at a 256 byte half page boundary. The starting address of display memory is placed in the Memory Controller's Video Base Address register by the Operating System or application. The Memory Controller will load display information into the Video Shifter 16 bits at a time, and the Video Shifter will decode this information to generate a serial display stream. In monochrome mode, each bit represents 1 pixel on or off. In color, bits are combined from each plane to generate the correct level of red, green, and blue.

For example, in low resolution (4 planes) 4 words are loaded into the Video Shifter for each word (16 pixels displayed on the screen. The Video Shifter combines bit 0 from each word to form a four bit number (0-15), and takes the color from the palette referenced by that number (e.g. 0101=5, use color from palette register 5) and outputs those levels, then takes bit 1 from each plane and outputs the color from the palette referenced by those four bits, etc.

Glue

Glue provides timing control to the Memory Controller, video output, and monitor/RF output. VSYNC input to the Memory Controller causes the starting address of the display memory to be reloaded into the address counter during vertical blanking. DISPLAY ENABLE (DE) tells the Memory Controller and Video Shifter that a display line is being scanned and data should be loaded into the Video Shifter. BLANK shuts off the video output from the Video Shifter during periods when the scan is not in a displayable part of the screen. VSYNC and HSYNC both go to the monitor output and RF modulator. These signals synchronize the monitor or T.V. vertical and horizontal sweep to the display signal.

Memory Controller

In addition to the inputs from Glue mentioned above, there are two output control signals associated with video. DCYC strobes data from display memory into the Video Shifter. CMPCS (color map select) is active only when changing the color attributes in the color palettes.

Sound Synthesizer

The YM2149 Programmable Sound Generator (PSG) produces music synthesis, sound effects, and audio feedback (e.g. alarms and key clicks). The clock input is 2 MHz; the frequency response range is 30 Hz to 125 KHz. There are three sound channels output from the chip, which are mixed and sent to the monitor speaker.

The PSG is also used in the system for various I/O functions relating to printer port, disk drive, and RS232.

Video Interface

The two types of interface are provided in the base ST's are analog RGB and monochrome. The STM and STFM versions have in addition composite and modulated RF outputs. The presence of a monochrome monitor is detected by the MONOMON input (when a monochrome monitor is connected, it will be low). The possible displays are:

Monochrome: single emitter follower amplifier driving the output of the Video Shifter.

RGB: resistor network sums outputs for each color. The three colors each have an emitter follower amplifier to drive output.

Composite (STM and STFM): the outputs of the emitter

followers are input to the modulator box, where the vertical and horizontal sync signals are added to form the composite signal.

Television (STM and STFM models): the composite signal is modulated onto an RF carrier. The signal is locked onto the color burst frequency by the phase locked loop (PPL). Without the PPL, the colors will shift or dance on the T.V. screen. The PPL was not included in the printed circuit design of early versions, and is a hand wired modification. On some versions of the 1040ST, the PPL is on a small daughter board just in front of the shield enclosing the Video Shifter.

Monitor Inputs:
Hsync—TTL level, negative, 3.3 k ohm.
Vsync—TTL level, negative, 3.3 k ohm.
Monochrome—digital 1.0V P-P, 75 ohm.
R,G,B—analog 0-1.0V P-P, 75 ohm.
Audio—1V. P-P, 1k ohm.

Monitor

1 — Audio Out
2 — Composite Video
3 — General Purpose Output
4 — Monochrome Detect
5 — Audio In
6 — Green
7 — Red
8 — Plus 12-Volt Pullup
9 — Horizontal Sync
10 — Blue
11 — Monochrome
12 — Vertical Sync
13 — Ground

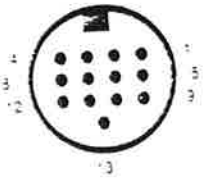


Figure 1.4
Monitor Port

Musical Instrument Communication

The Musical Instrument Digital Interface (MIDI) allows the integration of the ST with music sysnthesizers, sequencers, drum boxes and other devices possessing MIDI interfaces. High speed (31.25 Kilobaud) asynchronous current loop serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port). MIDI specifies that data consist of 8 data bits preceded by one start bit and followed by one stop bit.

Communication takes place via a 6850 ACIA. The CPU reads and writes to the 6850 in response to interrupts which are passed from the 6850 to the MFP interrupt controller. The system is interfaced to the outside via two inverters on the transmit side and an LED/photo-transistor chip on the input side. The input signal is routed around through two inverters to the output connector where it is called MIDI THRU in order to allow chaining of multiple devices on the MIDI bus.

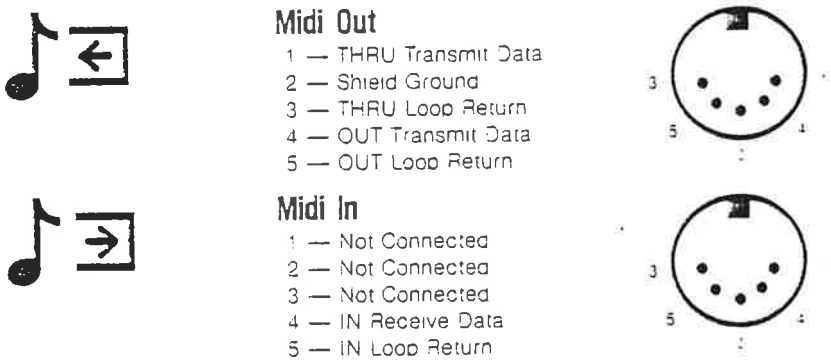


Figure 1.5
MIDI PORTS

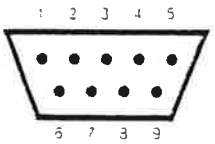
Intelligent Keyboard

The keyboard transmits make/break key scan codes, ASCII codes, mouse data, joystick data, in response to external events, and time-of-day data (year, month, day, hour, minute, second) in response to requests by the CPU. Communication is controlled on the main board by a 6850 device and on the keyboard assembly by the 1MHz 8 bit HD6301 Microcomputer Unit. The HD6301 has internal RAM and ROM. Included in ROM are self-test diagnostics which are performed at power-up and whenever the RESET command is sent over the serial communication line by the CPU. The MC6850 is read and written to by the CPU in response to interrupts which are passed to the CPU by the MFP interrupt controller.

The 2 Button Mouse is an opto-mechanical device with the following characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second and a maximum pulse phase error of 50 percent. The joystick/mouse port has inputs for up, down, left, right, right button, left button. The right button equals the joystick trigger, and the left button is wired to the second joystick port trigger. The joystick has four directions (up, down, etc.) and one trigger.

Mouse / Joystick

1 — Up/XB
2 — Down/XA
3 — Left/YA
4 — Right/YB
5 — Not Connected
6 — Fire/Left Button
7 — +5VDC
8 — Ground
9 — Joy1 Fire/Right Button



Joystick

1 — Up
2 — Down
3 — Left
4 — Right
5 — Reserved
6 — Fire Button
7 — +5VDC
8 — Ground
9 — Not Connected

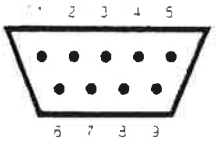


Figure 1.6
MOUSE/JOYSTICK PORTS

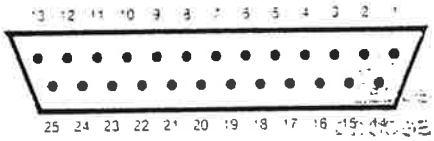
Parallel Interface

The parallel port is primarily intended as a Centronics type printer interface, but can also be used as a general purpose I/O port. Centronics STRCBE and BUSY are supported. BUSY is read by the MFP chip. Data and strobe signals are output by the YM2149 PSG chip. Not all Centronics printers are compatible with this port. The current loading on the data lines should not exceed 2.3 mA. (This corresponds to a 2.2k ohm resistor pull-up on the printer side.)

The port can be programmed to be input or output. The PSG chip is read directly by the CPU, with Glue doing address decode to provide chip select.

Printer

1 — STROBE
2 — Data 0
3 — Data 1
4 — Data 2
5 — Data 3
6 — Data 4
7 — Data 5
8 — Data 6
9 — Data 7
10 — Not Connected



11 — BUSY
12-17 — Not Connected
18-25 — Ground

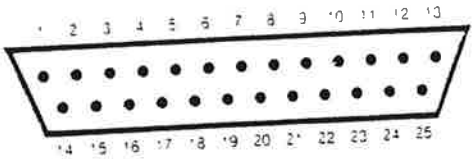
Figure 1.7
PRINTER PORT

RS232C Interface

The RS232C interface provides asynchronous serial communication with five handshake control signals: Request to Send and Data Terminal Ready are output by the PSG chip; Clear to Send, Data Carrier Detect, and Ring Detect are input to the MFP chip. The MFP contains a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) which handles dat transmission and reception. The 2.4576 MHz clock to the MFP is divided by the timer D (pin 16) output of the MFP to provide the basic clock for receiver and transmitter. Data rate of 50 to 19200 bits per second are supported. 1488 line drivers and 1489 line receivers with +/- 12v. supply meet the EIA RS232C standard for electrical interface.

Modem

1 — Protective Ground
2 — Transmitted Data
3 — Received Data
4 — Request to Send
5 — Clear to Send
6 — Not Connected
7 — Signal Ground
8 — Data Carrier Detect
9-19 — Not Connected
20 — Data Terminal Ready



21 — Not Connected
22 — Ring Indicator
23-25 — Not Connected

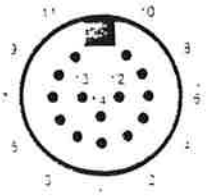
Figure 1.8
RS 232 PORT

Disk Drive Interface

The ST computers have a built-in floppy disk controller (a Western Digital 1772) and logic for selecting up to two single or double sided drives. The 1040 ST has one built-in floppy disk drive and provision for one external disk drive. The Western Digital WD1772 Controller services both drives. Drive and side selection is done by outputs on the YM2149 PSG chip. The CPU reads and writes to the 1772 through the DMA Controller. The 1772 interrupts the CPU on the INTR line, via the MFP interrupt controller. The 1772 accepts high level commands, such as seek, format track, write sector, read sector, etc. and passes data to the DMA Controller (see DMA controller under Main System, above, for details on DMA transfer). The 1772 interrupts the CPU when the operation is complete. The CPU is freed from much of the overhead of disk I/O.

Floppy Disk

1 — Read Data
2 — Side 0 Select
3 — Logic Ground
4 — Index Pulse
5 — Drive 0 Select
6 — Drive 1 Select
7 — Logic Ground
8 — Motor On
9 — Direction In
10 — Step
11 — Write Data



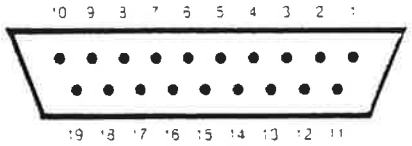
12 — Write Gate
13 — Track 00
14 — Write Protect

Figure 1.9
FLOPPY PORT

Hard Disk Interface

The hard disk drive interface is provided through the DMA controller; the hard disk controller is off-board and is board and is sent commands via an SCSI-like (Small Computer System Interface) command parameter block. Data is transferred via DMA. Writing to the external controller causes HDCS (Hard Disk Chip Select) to go low and CA1 to go high. DMA transfers are controlled by the external device. When data is available, or the device is ready to accept data, HDRQ will be driven high by the external controller. The DMA chip must respond within 250 nanoseconds with ACK (low) to acknowledge that data is on the bus or has been read from the bus. The Memory Controller feeds data to or accepts data from the DMA Controller. Transfers can take place at up to 1 Mbyte/second.

Hard Disk



1 — Data 0
2 — Data 1
3 — Data 2
4 — Data 3
5 — Data 4
6 — Data 5
7 — Data 6
8 — Data 7
9 — Chip Select
10 — Interrupt Request
11 — Ground
12 — Reset
13 — Ground
14 — Acknowledge
15 — Ground
16 — A1
17 — Ground
18 — Read/Write
19 — Data Request

Figure 1.10
HARD DISK PORT

After a RESET (power-up or reset button) the 68000 will start executing at the address pointed to by locations 4-7, which is ROM (Glue maps 8 bytes of ROM at FC0000-7 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM (FC0000-FEFFFF). The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse).
2. Read the longword at cartridge address FA0000. If the data read is a "magic number", execute from the cartridge (diagnostic cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations were previously written), initialize the memory controller, and continue running the application which was running before the reset if it was a warm start.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.
6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if succeeded.
12. If no boot disk, the 16k boot ROM version will prompt the user to insert the system disk. The full 192k version will bring up the desktop.

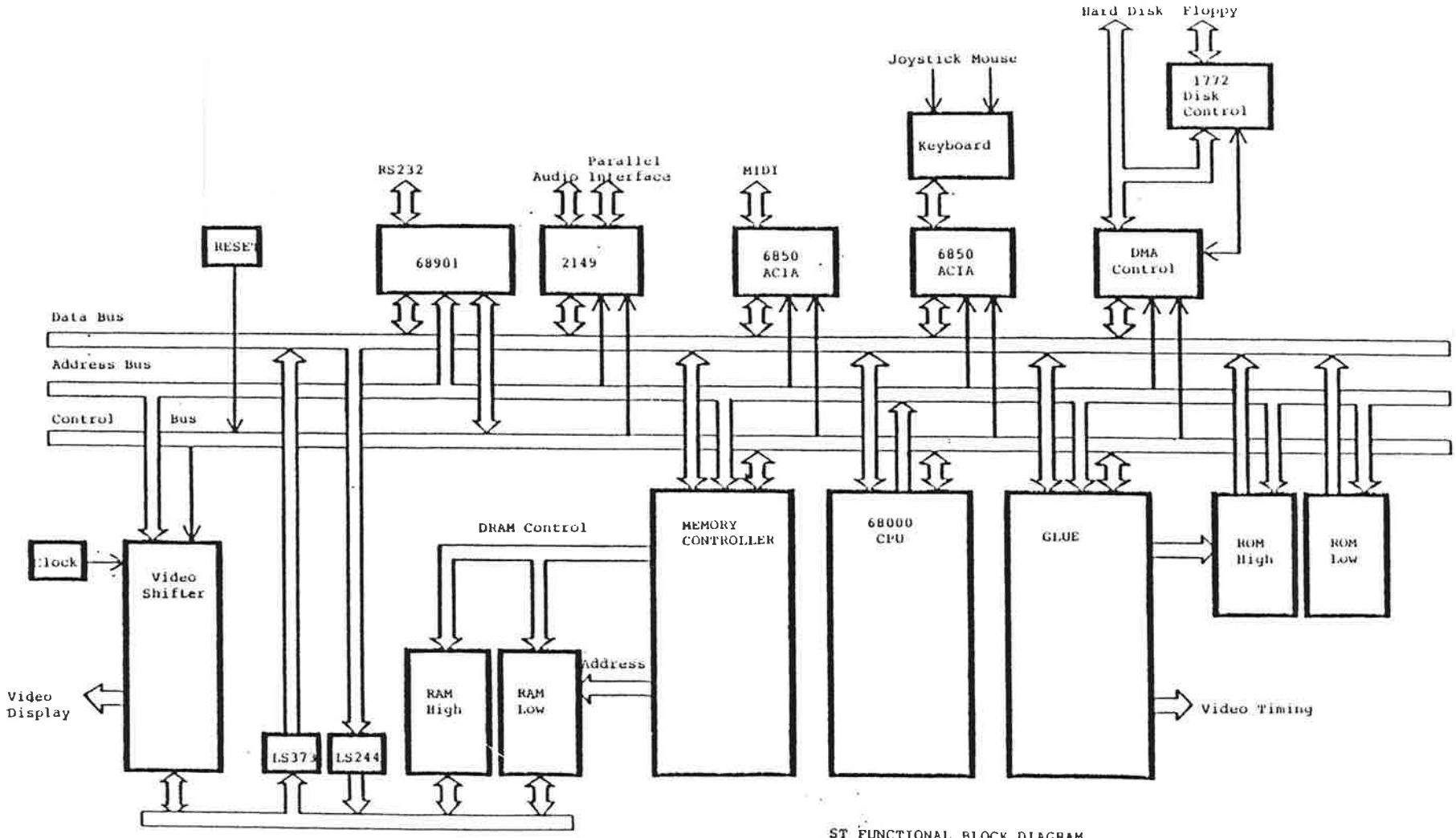
SYSTEM ERRORS

The 68000 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurances (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen (mushroom clouds in older versions of disk loaded operating system). The number of bombs equals the number of the exception which occurred.

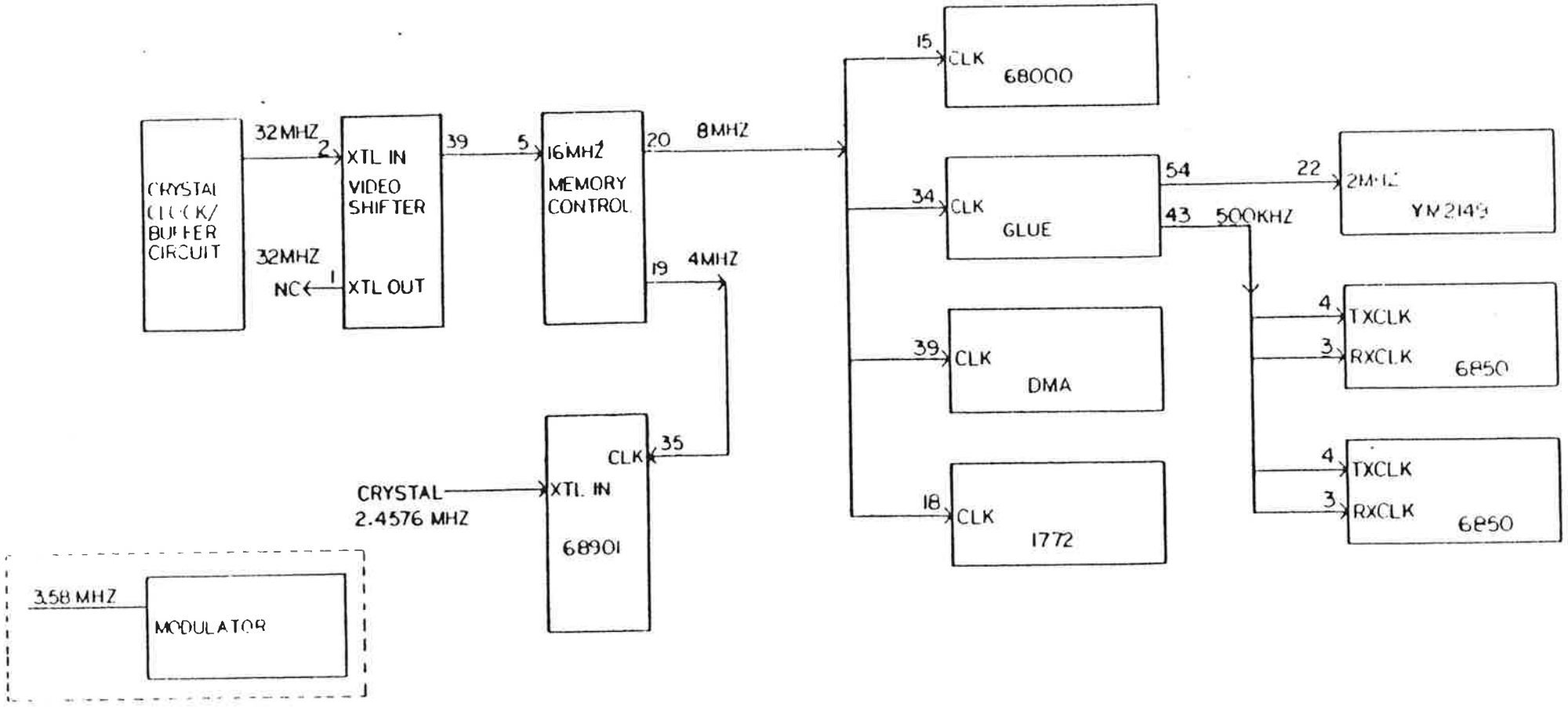
System errors may or may not be recoverable. Errors in loading files from disk will cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

Number of bombs and meaning
(Nos. 26,28,30, and 64-79 will not bomb, as they are legitimate.)

2 Bus Error. Glue asserted bus error or CPU detected an error.
3 Address Error. Processor attempted to access word or long word sized data on an odd address.
4 Illegal Instruction. Processor fetched an instruction from ROM or RAM which was not a legal instruction.
5 Zero Divide. Processor was asked to perform a division by zero.
6 Chk Instruction. This is a legal instruction, if software uses this, it must install a handler.
7 Trapv Instruction. See Chk instruction.
8 Priviledge Violation. CPU was in user mode, tried to access a location in supervisor address space.
9 Trace. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.
10 Line 1010 Emulator. CPU read pattern 1010 as an instruction. Provided to allow user to emulate his own instructions.
11 Line 1111 Emulator. See Line 1010 Emulator.
12-23 Unassigned, should be no occurrence.
24 Spurious Interrupt. Bus error during interrupt processing.
25-31 Autovector Interrupt. Even numbered vectors are used, others should have no occurrence.
32-63 TRAP Instruction. CPU read instruction which forced exception processing.
64-79 MFP interrupts.
80-255 User interrupts.



ST FUNCTIONAL BLOCK DIAGRAM



ST SYSTEM CLOCKS

SECTION THREE
TESTING

OVERVIEW

This section pertains to the test equipment, diagnostic software, and test procedures used to verify correct operation and repair the 1040 ST computer. The diagnostic cartridge should be used if possible. If the unit gives no display or RS232 output when running the cartridge, see "Troubleshooting a Dead Unit" below.

Since the level of complexity in the ST system is high, it should not be expected that this document can cover all possible problems or pinpoint the causes; rather, the intent here is to give a systematic approach which a technician can use to narrow down a problem to its most likely source. Experience in troubleshooting computer systems is assumed. Knowledge of the 68000 processor may be helpful. Economics will be an important consideration; due to the low cost of the ST computer line, little time can be justified in troubleshooting down to the component level when it may be cheaper to replace the entire assembly. Fortunately, many of the more expensive (and critical) components are socketed, making verification and replacement fast.

TEST EQUIPMENT

The following equipment will be needed to test the ST computer:

* Atari SC122 RGB Monitor (or similar)
* Atari SM124 Monochrome Monitor (or similar)
* Atari SF354 or SF314 Floppy Disk Drive
* ST Port Test Fixture
* RS232 Loop-Back Connector
* MIDI Loop-Back Cable
* ST Test Diagnostic Cartridge (Revision 3.5 or later)
* 2 Blank diskettes

In addition, the following items will be needed to troubleshoot and repair failed computers:

* 100MHz Oscilloscope
* Small Hand Tool Kit
* Spare Parts

TEST CONFIGURATION

Connect cables from test fixture into the hard disk port, parallel port, and joystick/mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the RS232 and MIDI loopback connectors into their ports. Plug a color monitor into the monitor output (monochrome can be used as a replacement) and insert the test cartridge (EPROMs face down). Power on the unit. Some test will be run automatically; in a few seconds the menu screen should appear. If the screen appears, skip down to "ST Diagnostic Cartridge", below. If not, read next section "Troubleshooting a Dead Unit".

TROUBLESHOOTING A DEAD UNIT

In the event that the system is correctly configured and powered and no display appears, this is the procedure to use for determining the problem. This assumes elementary steps have been taken, such as checking the LED in the forward left corner of the computer to verify the unit is powered and making sure the monitor is working.

1. Connect a dumb terminal to the RS232 port of the unit under test (U.U.T.), insert the Diagnostic Cartridge into the U.U.T., and power on the unit. If the Diagnostic Cartridge messages appear on the display of the terminal, use the diagnostic to troubleshoot the computer. If not, the computer will have to be disassembled to troubleshoot. Refer to "Diagnostic Cartridge" below and/or the Diagnostic Cartridge Troubleshooting Guide for information on using the cartridge.

If no activity is seen on the RS232 port or display, continue with (2) below.

The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity. Another Atari ST can be used as a terminal; use the VT52 emulator. (One of the menu selection under the DESK window in the GEM Desktop. You will need to boot the Desk Accessories files from disk to do this.) Use the default configuration.

2. Disassemble the computer so that the printed circuit board is exposed (see Section 4, Disassembly). Power up the computer. Using an oscilloscope, verify the 8MHz clock to the 68000 CPU. Replace oscillator if necessary. Then check pin 17 (HALT) of the 68000 CPU. It should be a TTL high. If so, go on to 3 below. If not, the CPU is halted. The reasons may be: (1) bad reset circuit, (2) double bus error, 3) bad CPU. Check (1) by observing signal on input of the two inverters on the HALT line. Check (2) by observing pin 22 of the CPU (BERR) as the unit is powered on. It should be high always. If there are logic low pulses, some component is malfunctioning and Glue is generating the error. Verify the clocks to Glue and Memory Controller and replace these

components to verify them. If still failing, the CPU is unable to read ROM or there is a component which is not responding to a read or write by the CPU, probably the MFP 68901 or DMA Controller. The MFP should respond to an MFPCS with DTACK. The DMA chip should respond to FCS by asserting RDY. There is no way to check (3) other than by elimination of the other two possiblities, although a hot CPU (too hot to touch for more than a second) strongly indicates a bad CPU.

3. If the CPU is not halted, it should be reading instructions from ROM (cartridge, if installed) and data and address lines will be toggling. (If not, replace CPU.) At this point, there is the possibility that both the video and RS232 subsystems are failing. Verify the output of the MFP chip (pin 8) while powering on the unit with the cartridge installed. If data is being sent, trace it through the 1488 driver. Note that + and - 12v. is required for RS232. If all looks good, there may be something wrong with the connection to the terminal.

Verify also the output of the Video Shifter. If using an RGB monitor, check the outputs to the summing resistors for R, G, and B. Note that if BLANK is not going high, no picture will be possible. If using monochrome, check output pin 30. Also check the input to the MFP, pin 29, MONOMON. Note that if the CPU does not read a low on this signal on power-up, it will cause RGB output on the Video Shifter.

If the Video Shifter is outputting a signal, but the picture is unreadable, there is probably a problem with screen RAM. The cartridge should be used to diagnose this problem, with the RS232 terminal as a display device.

ST DIAGNOSTIC CARTRIDGE

The ST Diagnostic Cartridge is used to detect and isolate component failures in ST computers (520 and 1040). There are several revisions; this document refers to revision 3.5. Users of earlier versions should refer to the appropriate Troubleshooting Guide. This section gives a brief guide to use with a description of each test; for more detail on troubleshooting, refer to the Troubleshooting Guide. Note that RAM failures in low memory require an RS232 terminal to troubleshoot (see below).

Power-up

The diagnostic program performs several tests on power-up. In particular, the message "Testing MFP, Glue timing, Video will appear, and the screen will appear scrambled for a few seconds before the menu is printed. The screen will turn red (dark background in monochrome) if an error occurs in the initial testing, with a message indicating the failure. The lowest 2 Kbytes of RAM is tested on power-up; if a location fails, the error will be printed to the RS232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there is no stack or system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen may turn red). Repair RAM.

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS232 port. The diagnostic program looks for keystrokes from the RS232 device. The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity. Another Atari ST can be used as a terminal; use the VT52 emulator. (One of the menu selection under the DESK window in the GEM Desktop. You will need to boot the Desk Accessories files from disk to do this.) Use the default configuration.

If the display is unreadable, the RS232 terminal should be used. All messages are printed to the RS232 port as well as the screen.

Test Menu

The normal screen will be dark blue with white letters. The title and revision number are displayed at the top, with the amount of RAM below, and a test menu below that. To select tests, the user types the keys corresponding to those tests, and then the return key. Many iterations of the test or tests chosen can be run by typing in the number of cycles just before typing RETURN. Typing a zero will cause the test sequence to run continuously. To stop a cycle before completion, hit the escape key (there may be some delay in some tests before the test stops). As each cycle completes, the total numbers of cycles will be displayed on the screen.

Below the test selections are four options:

* Install disk drive--specifies the floppy drives to test

* Run All Tests--runs all tests except the ones which require operator interaction.

* Examine/Modify memory--allows user to read and modify memory locations in the ST, including hardware registers.

* Help--gives brief explanation of some features of the program.

Summary of Tests

RAM--tests in three stages: low 2 kbytes, middle (up to 64k), and 64k to top. Writes all 1s, all 0s, counting pattern (data=address low word), reverse counting pattern (data= complement of address low word). Finally, checks addressing at 64k boundaries by writing unique pattern in last 256 bytes of each 64k block. An error causes the address to be displayed, followed by the data which was written and data which was read.

ROM--reads all bytes from operating system ROMs and calculates the checksums. Compares against known values of checksums and determines if good or bad.

COLOR--verifies the Video Shifter. Seven color bands are displayed: red, green, blue, cyan, magenta, yellow, and white. Each band consists of 8 levels of intensity. All 16 color palettes are represented, each palette is a vertical strip across the screen. The offset at the right edge of the screen is the border between palette 15 and palette 0 (border palette). All 16 palettes are written to during a scan line, by the time the 16th palette is displayed, the first palette has been written with the next color, so when the scan gets to the border, the next color is displayed.

The operator should see that there are no gaps or missing scan lines in the display. If lines are missing, check the three outputs on the Video Shifter for that color, and verify the values of the resistors on the output. Too low a brightness setting on the monitor will cause the monitor not to distinguish between fine levels, making it appear there are only four levels being output.

KEYBOARD--two types of test are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. The operator presses keys and observes that the corresponding character on the screen changes (reverses background color). If multiple tests have been selected, only the self-test is run.

The self-test checks communication between the CPU and the keyboard microcomputer, and checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

MIDI--sends data out the MIDI port, (data loops back through the

cable) and reads from the input and verifies the data is correct. This also tests the interrupt from the 6850 through the MFP chip.

SERIAL RS232--tests the RS232C control lines (which are tied together by the loopback connector) and data loopback. Checks data transmissing/receiving using polling method first, then using interrupts. Data is transmitted at 300, 600, 1200...19200 bps. Data transmission is performed by the MFP and the 1488 and 1489 driver and receiver chips. Interrupts are a function of the MFP. Control lines are output by the PSG chip and input on the MFP. Note that this test does not thouroughly test the drive capability of the port. If the test passes, but the unit fails in use, it is likely that the 1488 or 1489 chips are bad.

AUDIO--outputs low to high sweep on each of the three sound channels. If single test is selected, the test will repeat continuously until a key is pressed. In mutiple test mode, only one test is performed. If a channel is missing, replace the PSG chip. If no sound is heard, verify the output of the chip with an oscilloscope, and trace the signal to the monitor output connector. If no output from the PSG, verify the PSG is being selected by running the printer port or RS232 test.

TIMING--this test is run on power-up as well as being selectable from the menu. The MFP timers, the Glue timing for VSYNC and HSYNC, and the Memory Controller video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as this test is run.

DMA PORT--writes four sectors (2048 bytes) of data to the RAM on the port test fixture via high speed DMA, reads it back, and verifies the operation was performed correctly.

FLOPPY DISK--for each disk installed, formats, writes, and reads tracks 0, 1, and 79 of side 0. If double sided, formats and writes track 79 of side 1 and verifies that side 0 was not overwritten. If no disks are installed, checks to see what drives are online and if they are double or single sided. To assure that the drive are correctly tested, the operator should install (menu option) before calling the test. Once the test is run, the drives become installed, and will be displayed on the menu screen (below the RAM size).

PRINTER/JOYSTICK--uses the port test fixture to test parallel printer port and joystick ports. Parallel port test writes to a latch on the test fixture and reads back data. Joystick port test outputs data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU.

HIGH RESOLUTION MONITOR--when this test is selected, a message is displayed to connect the monochrome monitor. The CPU waits for an interrupt from the MONOMON input to the MFP, and when received

(the operator connects the monochrome monitor), changes the display to high resolution. The display screen shows horizontal and vertical lines, each 2 pixels in width. When the operator sees the display is correct, he unplugs the monochrome monitor and re-connects the RGB monitor and the display should return to normal.

ERROR CODES QUICK REFERENCE

This is a very brief summary of all error code which may occur when running the diagnostic. All errors are explained in greater detail in the Diagnostic Cartridge Troubleshooting Guide.

INITIALIZATION (Errors occuring before the title and menu appear.)

I1 RAM data line is stuck.
I2 RAM disturbance. Location is altered by write to another location.
I3 RAM addressing. Wrong location is being addressed.
I4 MMU error. No DTACK after RAM access.
I5 RAM sizing error. Uppermost address fails.

EXCEPTION (may occur at any time)

E1—E5 not used
E6 Autovector error. IPL0 is grounded or 68000 is bad.
E7 Spurious interrupt. Bus error during exception processing.
E8 Internal Exception (generated by 68000).
E9 Bad Instruction Fetch.
EA Address error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceeded by a bus error or bad instruction fetch.
EB Bus error. Generated internally by the 68000 or externally by Glue. Usually caused by device not responding. Displays the address of the device being accessed.

RAM

R0 Error in low memory, possibly affecting program execution.
R1 Error in RAM chip.
R2 Address error. Bad RAM chip or memory controller. Address line not working.
R3 Address error at 64k boundary.

KEYBOARD

K0 Stuck key
K1 Keyboard controller is not responding.
K2 Keyboard controller reports error.

MIDI

M0 Data not received.
M1 Data received is not what was sent.
M2 Data input framing error.
M3 Parity error.
M4 Data overrun. Byte was not read from the 6850 before next byte arrived.

RS232

S0 Data not received.
S1 Data received is not what was sent.
S2 Data input framing error.
S3 Parity error.
S4 Data overrun. Byte was not read from the MFP before the next

byte arrived.

S5 IRQ. The MFP is not generating interrupts for transmit or receive.

S6 Transmitter error--MFP.

S7 No interrupt from transmit error (MFP).

S8 No interrupt from receive error (MFP).

S9 DTR--RI. These signals are connected by the loopback connector. Changing DTR does not cause change in RI.

SA DTR--DCD. Same as S9 for these signals.

SB RTS--CTS. Same as S9 for these signals.

DMA

D0 Time-out. DMA did not take place, or interrupt not detected.

D1 DMA count error. Not all bytes arrived. Possible Memory Controller error.

D3 DMA Controller not responding.

TIMING

T0 MFP timers failed.

T1 Vertical sync timing failed.

T2 Horizontal sync timing failed.

T3 Display Enable Interrupt failed.

T4 Memory Controller video address counter failed.

PRINTER AND JOYSTICK PORTS

P0 Printer port error.

P1 Busy (printer port input) failed.

J0 Joystick port 0 failed.

J1 Joystick port 1 failed.

J2 Joystick (keyboard controller) timed-out.

J3 Left button line failed.

J4 Right button line failed.

FLOPPY DISK DRIVE

F0 Drive offline. Not responding to restore (seek track 0).

F1 Format error.

F2 Write error.

F3 Read error.

F4 Seek erro.

F5 Write protected.

F6 Data compare. (Data read not equal to data written.)

F7 DMA error.

F8 DMA count error (Memory Controller counter.)

F9 CRC error.

FA Record not found.

FB Lost data.

FC Side select error.

SECTION FOUR
DISASSEMBLY/ASSEMBLY

1040ST DISASSEMBLY

Use the following procedure to disassemble the 1040ST. Refer to Assembly Drawing, Section 6.

Top Cover/Keyboard Removal

1) Turn unit upside down.

2) Remove the 7 screws from the square holes. These fasten the top case to the bottom. If the printed circuit board is to be exposed, or the disk drive is to be removed, also remove the three screws from the round holes. These hold the disk drive in place.

3) Turn the unit upright and remove the top case.

4) Remove the keyboard by unplugging the keyboard harness connector located in the right front corner.

Disk Drive Removal: lift the disk drive slightly and unplug the power harness connector and the ribbon cable.

Power Supply Removal (the power supply may be left in place and the upper shield removed in one piece for troubleshooting):

1) Remove one screw on the right side of the power supply shield.

2) Straighten the two twist tabs.

3) Lift off the power supply shield from the rear.

4) Unplug the wire harness connector in the right front corner of the power supply.

5) Remove two screws at front corners of power supply.

6) Lift the power supply up out of the main assembly.

Removal of main assembly from bottom case:

1) Remove four screws from the front of the shield/ printed circuit board assembly.

2) If power supply has not already been removed, remove two screws securing the power supply to the case at the front corners of the power supply. This can be done by inserting a screwdriver through the holes in the power supply shield or

by removing the shield.

3) Lift the assembly up from the front and pull forward.

Removal of Shield From Printed Circuit Board:

1) Straighten ten twist tabs.

2) Remove copper tape (if present).

3) Lift upper shield staight up.

Note: now that the major components are exposed, this is a convenient configuration for troubleshooting. The keyboard and disk drive may be re-connected and placed off to the side if those components are needed.

4) Lift printed circuit assembly away from bottom shield. It may be necessary to pull the twist tabs away from the board slightly.

1040ST RE-ASSEMBLY

1) Place insulation panel on Bottom Shield.

2) Place Main Board on top of Bottom Shield over insulator panel.

3) Plug in power supply connector and position power supply with tabs in slots.

4) Align tabs on bottom shield with slots on top shield and fit top shield over main assembly. Twist the tabs to lock in place.

5) Place assembly in lower plastic case.

6) Fasten the power supply to the bottom case at both front corners with two screws. This can be done with the power supply shield in place, using a magnestized screwdriver to hold the screw, or by removing the shield.

6a) If power supply shield was removed from main shield, position it over the power supply. Front tabs slide under slots. Twist rear tabs and replace the screw.

7) Plug disk drive power and ribbon cables into drive (cables go under shield), and position drive over standoffs.

8) Replace four screws at the front edge of the main assembly.

9) Connect Keyboard Harness to Main Board through the opening in the upper shield, and place keyboard on the supporting ribs of the bottom case.

10) Place the top cover over the assembly.

11) Turn over the assembly and replace the ten screws. The three longer screws go in the round holes to secure the disk drive.

WORD OF CAUTION

It is strongly recommended that the computer be retested once in plastic to make sure that the re-assembly was done correctly and there are no shorts to the shield.

520ST DISASSEMBLY

1) Turn unit upside down.

2) Remove the 6 screws from the bottom case.

3) Turn unit upright and remove top case.

4) Remove keyboard from main assembly by unplugging the connector from the right front of the assembly.

5) Remove the 3 screws from the front edge of the printed circuit board, and 3 screws from the rear edge of the printed circuit board (accessed through holes in the metal shield).

6) Remove the printed circuit board assembly from the bottom case.

7) Straighten the ten twist tabs around the edges of the assembly, and remove the top shield.

8) The printed circuit assembly is now exposed. The bottom shield can be removed if needed.

520 ST RE-ASSEMBLY

1) Place insulation sheet on bottom shield.

2) Align the twist tabs so that they will fit through the slots in the printed circuit assembly, and place printed circuit assembly on the bottom shield.

2a) It may be easiest at this point to place the assembly in the bottom case and screw in the 3 screws at the rear before the top shield is put in place. If a magnetized screwdriver or other device can be used to hold the screws in place while inserting them through the holes in the shield, skip this step.

3) Place the top shield over the assembly and twist the tabs to secure in place.

4) Place the shield/board assembly into the bottom case (if not already done in step 2a) and screw in 3 screws at the rear through the holes in the shield, and 3 screws at the front of the printed circuit board.

5) Plug the keyboard connector into the printed circuit board through the hole in the shield in the right front corner and position the keyboard in place on the lower case.

6) Place the upper case over the assembly, turn the unit over, and replace the 6 screws in the bottom case (the longer screws go in the rear).

SECTION FIVE
SYMPTOM CHECKLIST

This section gives a brief summary of common problems and their most probable causes. For more detail, refer to the section on troubleshooting in this document, or the Diagnostic Cartridge Troubleshooting Guide.

DISPLAY PROBLEMS

Symptom	Probable cause
Black screen	No power (check LED), bad Glue chip, bad Video Shifter. See TESTING section, "Troubleshooting a Dead Unit".
White screen	Video Shifter, Glue, Memory Controller, DMA Controller, 68000. Use diagnostic cartridge with terminal connected via RS232 port.
Dots/bars on screen	RAM, Memory Controller, Video Shifter. Use diagnostic cartridge.
One color missing	video summer, buffer, Video Shifter. Check signals with oscilloscope.
Scrambled screen	Glue, Memory Controller. Use diagnostic cartridge.
T.V. output bad	Modulator, phase locked loop. Trace signal with oscilloscope.

DISK DRIVE PROBLEMS

Disk won't boot	Power supply, 1772, DMA Controller, PSG chip, disk drive. See if select light goes on, if not, check PSG outputs. Listen for motor spinning. If not, check power supply. Swap disk drive or try external drive (if testing 1040). If not working, check DMA Controller, 1772 with diagnostic cart.
Disk won't format	1772, DMA Controller, disk drive.
System crash after loading files	Diskette, disk drive, 1772, DMA, or Memory Controller. Swap diskette, retry. Use diagnostic cartridge to check 1772, DMA Controller, Memory Controller; replace disk drive.

KEYBOARD PROBLEMS

Bad keyboard, 6850, MFP.

MIDI PROBLEMS

Bad opto-isolator chip, 6850, inverter (74LS04, 74LS05).

RS232 PROBLEMS

Bad 68901 MFP, receiver, driver, or PSG chips, +/- 12v power supply.

PRINTER PORT PROBLEMS

Bad PSG, MFP chips.

HARD DISK PORT PROBLEMS

Bad DMA Controller, Memory Controller, 1772 (loading the bus).

SECTION SIX
DIAGNOSTIC FLOWCHARTS

This section summarizes in diagramatic form the steps taken in troubleshooting the ST using the diagnostic cartridge. The details of using the cartridge are not shown; this shows the context in which the cartridge would be used, including some problems for which the cartridge would not be useful. Usage of the cartridge is covered in the troubleshooting guide. In general, the user would run all the tests, look up errors in the troubleshooting guide, and take the action recommended.

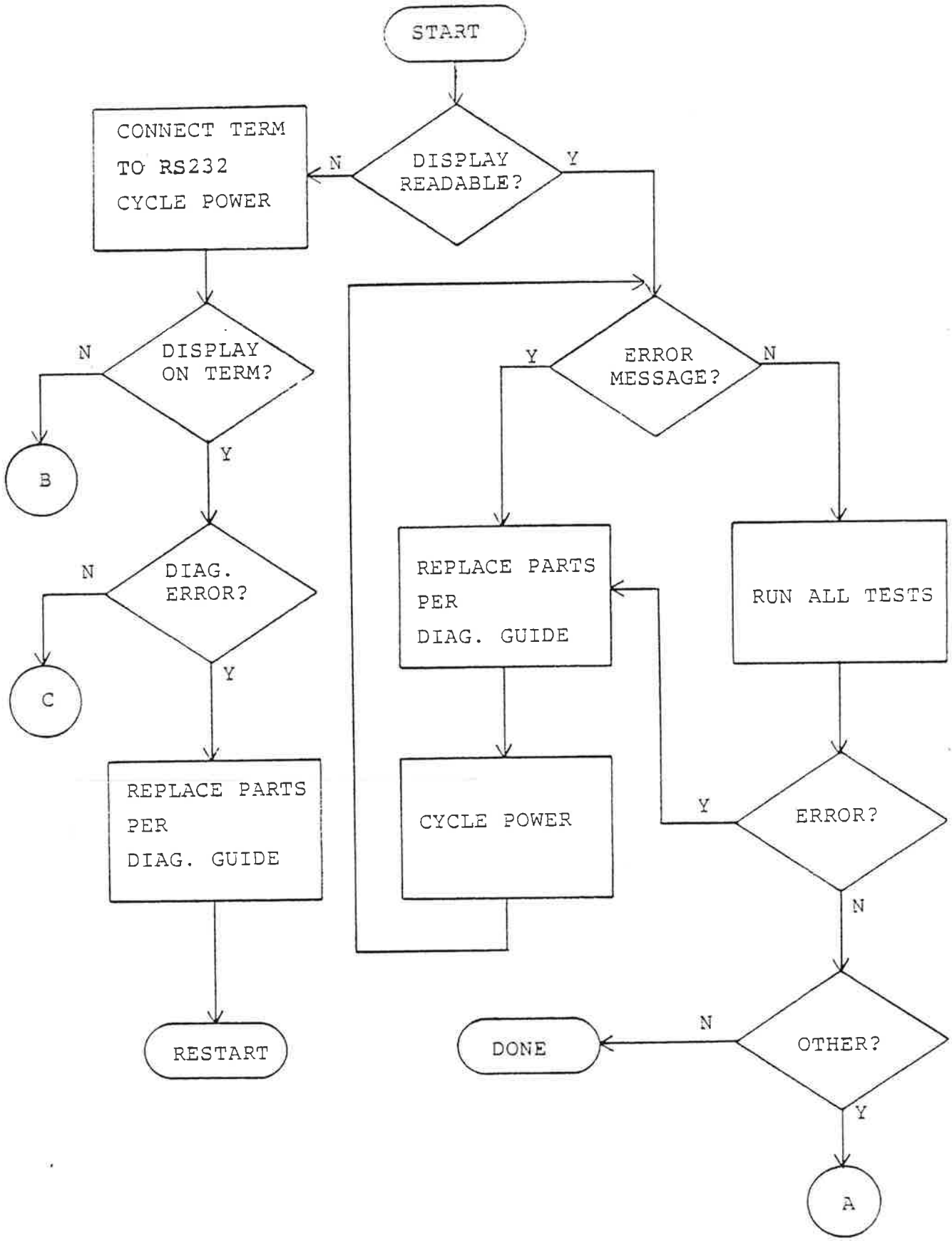
Although a thorough understanding of the system may be necessary in solving some problems, in most cases following the flowchart, reading the documentation on the diagnostic cartridge where necessary, and swapping out the indicated components will result in repair of the problem.

Replacement Procedures

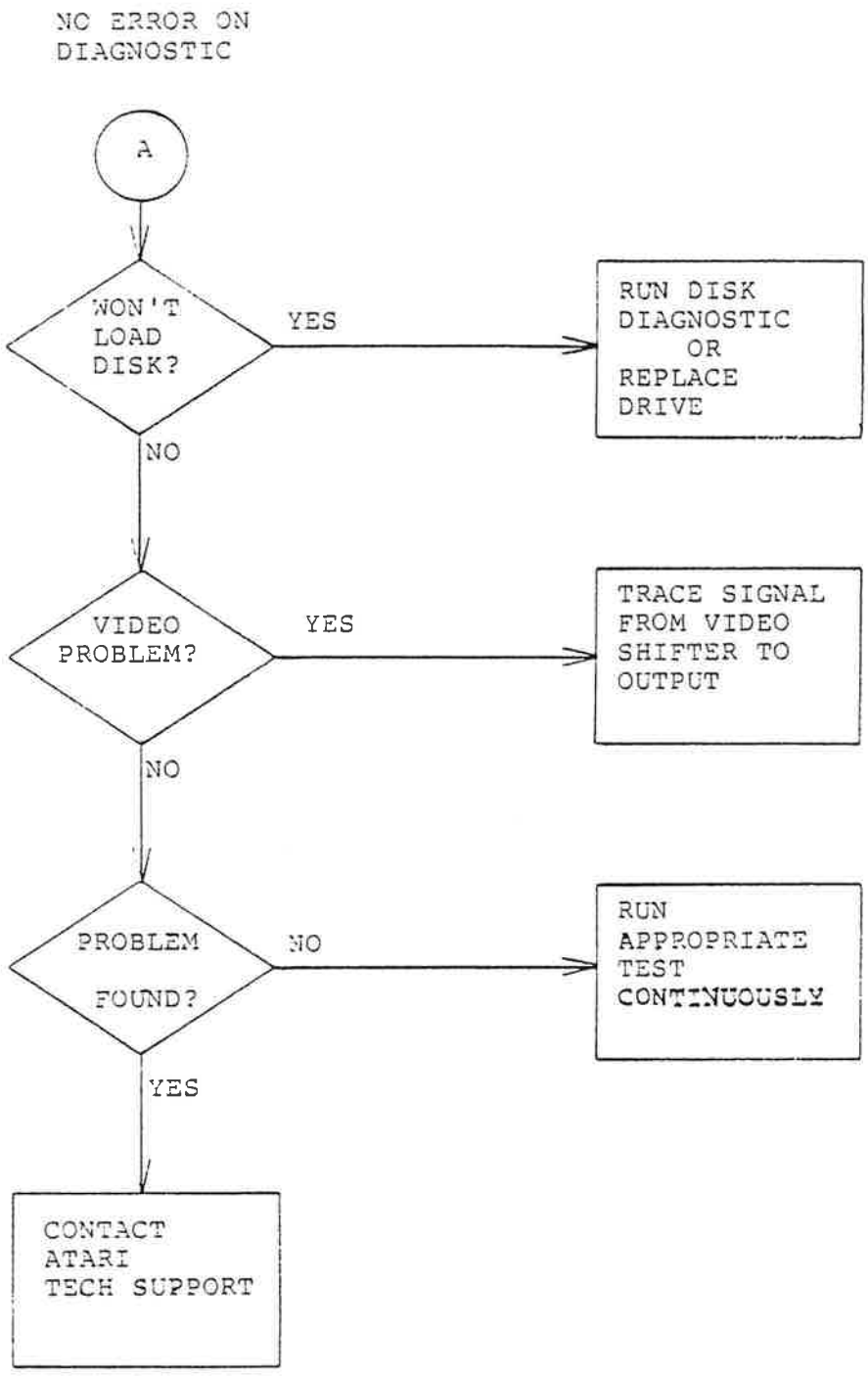
Where replacement is indicated, replace the component (if more than one is indicated, replace one at a time) with a known good part. If other components are later replaced, verify whether the first part is good by replacing in the system once the system has been repaired.

Handling of Integrated Circuits

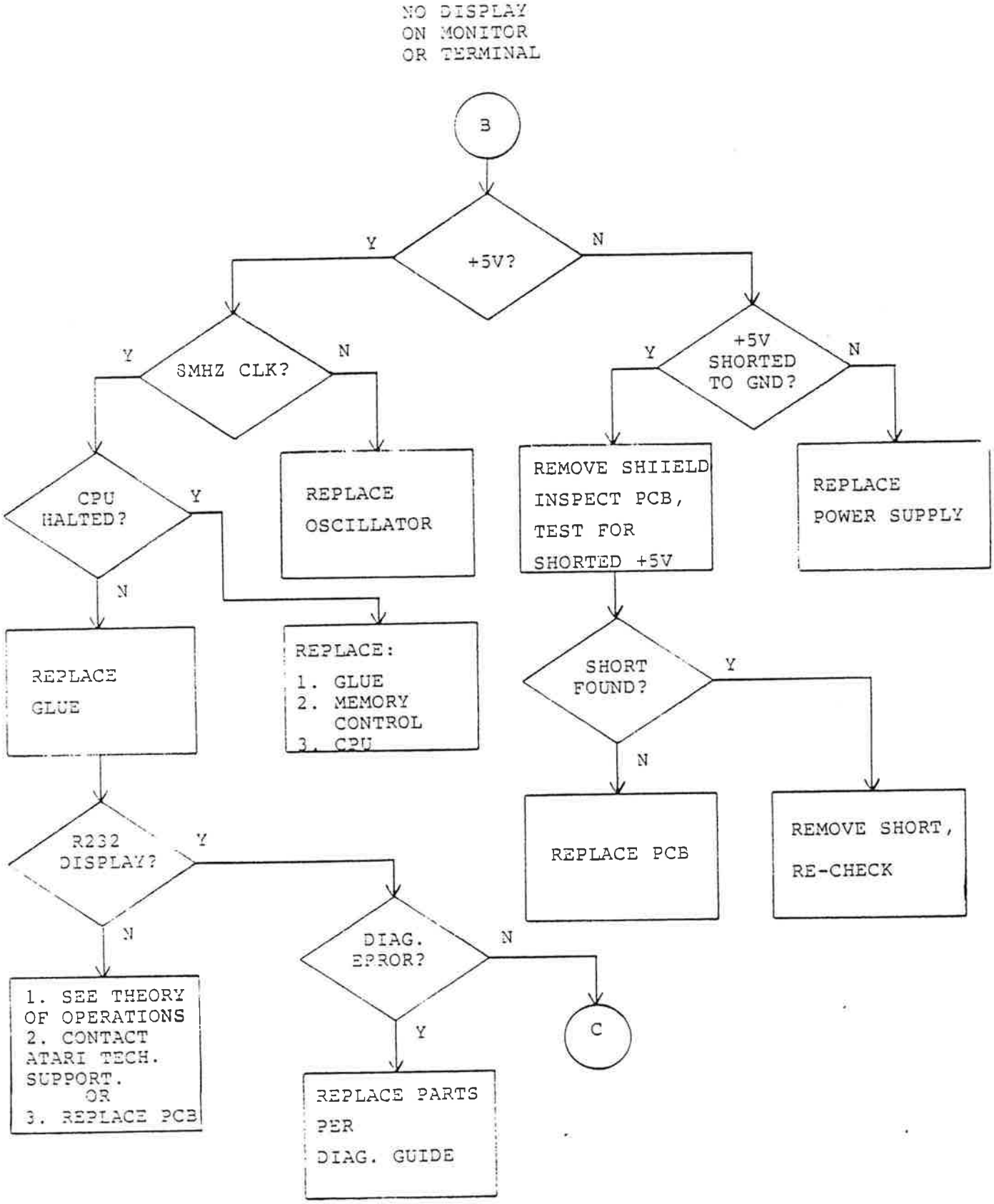
Extreme care should be taken when handling the integrated circuit chips. They are very sensitive to static electricity and can easily be damaged by careless handling. Keep chips in their plastic carriers or on conductive foam when not in use.



ST DIAGNOSTIC FLOW CHART 6.2

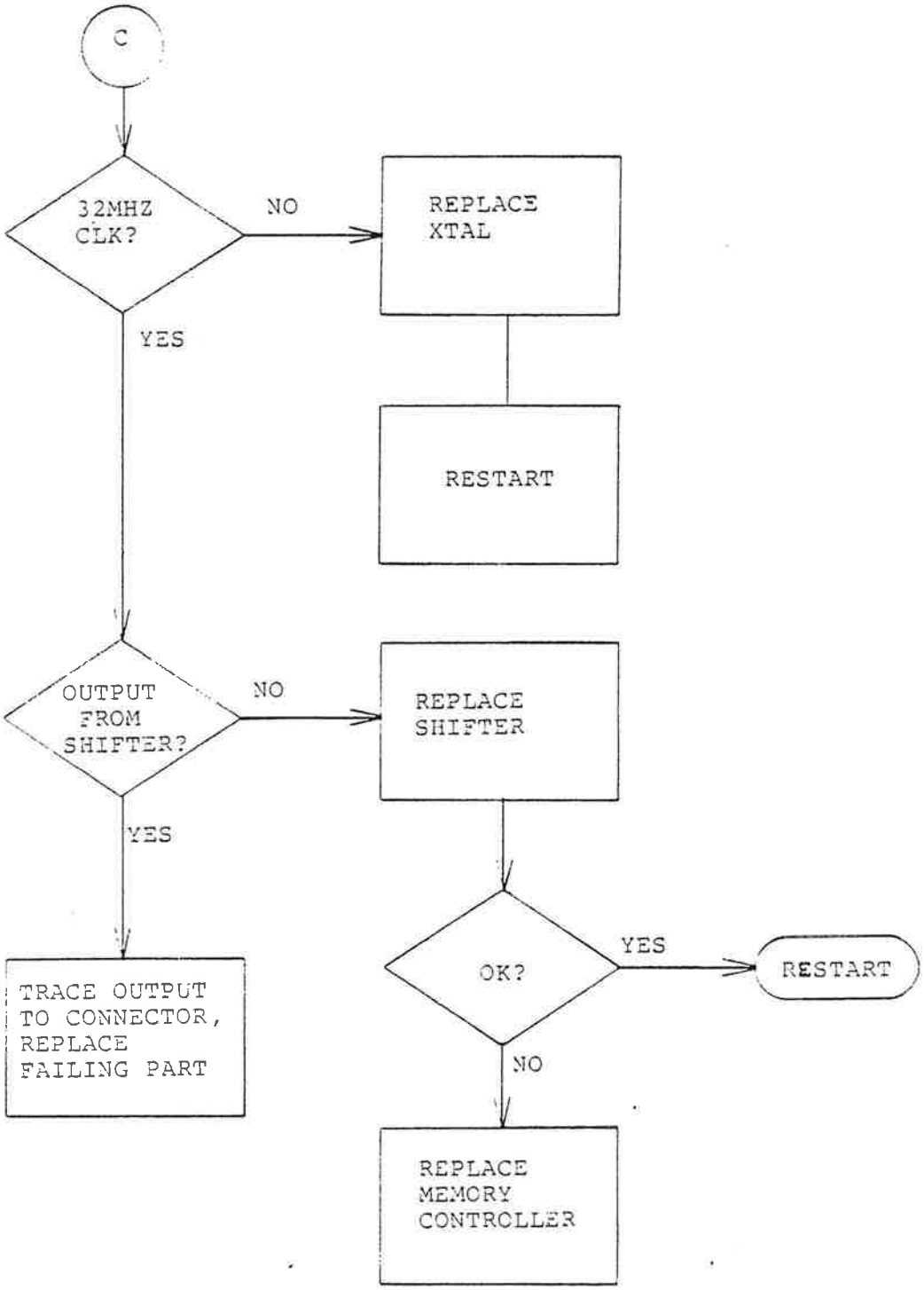


ST DIAGNOSTIC FLOW CHART 6.3



ST DIAGNOSTIC FLOW CHART 6.4

NO DISPLAY,
NO ERROR



ST DIAGNOSTIC FLOW CHART 6.5

CONTENTS

SECTION NINE
GLOSSARY OF PART NAMES AND TERMS

BUS ERRCR—Glue has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.

CPU—the 68000 microprocessor.

DMA—direct memory access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, takes place independent of the CPU, so the CPU can be processing while DMA is taking place. Glue arbitrates the bus between the CPU and DMA.

DMA CONTROLLER—Atari proprietary chip which controls the DMA process. All disk I/O goes through this device.

EXCEPTION—a state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also Section Two, System Errors, or a 68000 reference for more detail.

GLUE—Atari proprietary chip which ties together all system timing and control signals.

HALT—state in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bi-directional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert HALT.

HSYNC—timing signal for the video display. Determines when the

horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) also is encoded onto IPL1,2 as an interrupt to the CPU.

INTERRUPT--a request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities: the highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and Glue.

MEMORY CONTROLLER--Atari proprietary chip which handles all RAM accesses. See Theory of Operation, Main System and Video Subsystem for details.

MIDI--Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the 1040ST, consists of a 6850 communications chip, driver and receiver chips (74LS04, 74LS05, and PC-900 photocoupler), and an MFP interrupt channel.

MFP--Multi-function Peripheral, also 68901. Interrupt control, timers, and USART for RS232 communication. See Theory of Operation, Main System.

MODULATOR--device which combines video signals R,G,B, VSYNC, and HSYNC into a composite signal for monitors requiring this type input, and also modulates this signal, combined with audio, onto an RF carrier for output to a television.

PHASE LOCKED LOOP--circuit which locks the horizontal sync signal onto the color burst reference frequency for accurate color on the T.V. Without this circuit, colors on the T.V. become unstable, flickering or shifting about on the screen. The PPL may be on a daughter board located in front of the video shield or hand wired onto the main board within the video shield, or (possibly) in later versions, integrated into the printed circuit board.

PSG--Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.

RS232C--Electical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the ST computers, consists of the MFP, PSG, 1488, and 1489 chips.

1772--Western Digital Floppy Disk Controller.

6850--also ACIA (Asynchronous Communication Interface Adapter). Interfaces between 8 bit parallel bus and serial communication bus. In the ST, there are two 6850s, one for keyboard communication, and one for MIDI communication.

68901--see MFP.

SUPERVISOR MODE--state of the CPU in which it is allowed to access all hardware and RAM locations, and perform some priviliged instructions. Determined by the state of a bit in the Status Register. The operating system operates in supervisor mode, and switches to user mode before passing control to an application (although the application can enter supervisor mode if it wishes).

USER MODE--state of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.

VSYNC--signal used for vertical synchronization of CRT display device. Occurs at 70 Hz (monochrome), or 50 or 60 Hz color.

YM2149--see PSG.

ST DIAGNOSTIC CARTRIDGE TROUBLESHOOTING GUIDE

For REVISION 3.5

SCOPE

This document is intended as a guide for service technicians at authorized Atari Service Centers for using the ST Diagnostic Cartridge to troubleshoot the ST line of computers down to the component level.

Additionally, the diagnostic can be used by someone, not necessarily trained in servicing Atari computers, to verify the functionality of the computer.

Some familiarity with the ST computer is assumed. The ST Field Service Manual contains diagrams showing how to connect the test equipment, schematics, some information about using the test cartridge, general theory of operation for the ST, and guidelines on troubleshooting a dead unit (when the diagnostic cartridge cannot be used).

EQUIPMENT

At a minimum, you will need:

*Test Cartridge
*Monitor (RGB is recommended) or RS232 terminal (this can be an ST running the VT52 terminal emulator)
*Power supply

This much will allow you to test basic functions such as RAM, ROM, timing, and keyboard.

In addition, to test any of the I/O, you will need:

*ST test fixture with DMA port, printer port, and joystick port cables
*MIDI loopback cable
*RS232 loopback connector
*Monochrome monitor
*disk drives (1 or 2 may be tested, double or single sided)
*diskettes (appropriate type for drive being tested)

SETUP

With the power switch off, install the Diagnostic Cartridge (IMPORTANT—if not using plastic enclosed cartridge, BE SURE CARTRIDGE IS INSTALLED WITH CHIPS FACING DOWN) and connect cables for Joystick, Printer Port, DMA, and monitor, and install RS232 and MIDI connectors. J11 on the test fixture connects to Joystick 0 port. Turn power on.

TESTING

After turning power on, some initial tests will be run ("Testing MFP, Glue Timing, Video" will display briefly), and one of the following conditions will apply:

I. NO DISPLAY—verify power (see red LED in lower left corner of keyboard). If power is okay, turn off machine, remove RS232 loopback, and connect an RS232 terminal (you can use an ST running VT52 terminal emulator. See owner's manual for setting up VT52). The cable should connect pin 2 (serial out) of the unit under test to pin 3 (serial in) of the terminal, and vice versa. Connect pin 7 (ground) to pin 7. The device communicates at 9600 bps, 8 bits of data, no parity (use default set-up on VT52 emulator).
Turn the machine on again. Some messages should appear on the terminal (error codes or normal menu screen). If not, see the Field Service Manual, Section 5 for troubleshooting. A critical component, such as the processor, clock, or Glue is malfunctioning and must be repaired before the cartridge can be used.

II. DISPLAY APPEARS, RED SCREEN (ERROR)—find error code under STARTUP SEQUENCE below and follow the instructions for troubleshooting. If the error is in the keyboard, or the messages are not readable, you may want to connect an RS232 terminal (or ST running VT52 terminal emulator). See NO DISPLAY above for info on connecting a terminal. Reset the computer after connecting the RS232 device.

III. DISPLAY APPEARS, BLUE SCREEN—this is the normal condition. The display will show (for a 520 ST, others will show different amounts of memory):

```
            ST Diagnostic Test Rev. 3.5
520k RAM

R RAM           O O.S. ROM
C Color         K Keyboard
M MIDI          S Serial RS232
A Audio         T Timing
D DMA port      F Floppy Disk
P Print/Joystick ports
H High resolution monitor

I Install disk drive
Q Run all tests
E Examine/Modify memory
? Help

Enter letter(s) and RETURN
```

The operator selects the tests to run by typing the first letters of the tests. When the tests have been selected, the number of cycles is entered, and the RETURN key is pressed. If no number is entered, 1 pass is assumed. If 0 is entered, the test routine will run continuously until the ESC key is pressed. Examples:

D,RETURN	The DMA test will be run once.
R,S,M,RETURN	RAM, Serial, and MIDI tests will be run once.

M,5,RETURN The MIDI test will be run 5 times.
Q,0,RETURN All tests (except high resolution) will be run until the operator interrupts by pressing the ESC key.

Some tests perform differently when multiple tests or multiple cycles of one test are chosen, so that the operator can let the test run by itself without having to take any action. The keyboard test, in single cycle mode, displays a full keyboard, and as the operator presses each key, displays the key in inverse video. When multiple cycles are chosen, the keyboard self-test is performed. The color test runs until a key is pressed in single test mode, and runs for a fixed period of time in multiple test mode. The audio test outputs three sweeps (low to high frequency sound) in multiple test mode, one for each of the three sound channels, but will run until a key is pressed in single test mode.

TROUBLESHOOTING

Use this guide to locate faulty components after an error has been found by the test cartridge. Look under the section for the test which failed and find the error. (Some tests have no error messages; the user determines if the test fails. i.e., color, audio, high resolution.) You will find a short description of the test and a list of possible faulty components or a procedure to follow to further diagnose the problem. A general understanding of microprocessor systems is helpful, but often the problem can be solved by just replacing the recommended component. To save time and minimize damage to the PC board, swap out the socketed parts before replacing the soldered parts unless you are certain which part is bad. Also, verifying signals with an oscilloscope may be considered optional, as it is often quicker to change a part (if socketed) than trace down a signal. Try the easiest fix first.

Problems can sometimes be caused by improper seating of ICs (especially the square ICs), or shorting of components to the shieding, or loose bits of metal. After finding a problem, remove the plastic case and metal shield, and visually inspect the board. Check the seating of socketed parts. Test the unit again, before replacing any components. If the same problem occurs, go ahead and replace the components.

Some components will fail only at high temperature. If you are not able to reproduce a problem, it may be necessary to allow the unit to warm up, or to heat the components to speed up the failure. In cases where the problem is not immediate and obvious, it will be necessary to run the unit at temperature after replacing the suspected bad component to verify that the problem was solved. Cycle the test continuously.

In the following, references are made to the LSI (Large Scale Integration) parts. Refer to the part list and/or schematic to find the locator and part number for these devices:

Glue, DMA Controller, Memory Controller, 68901 Multi-function

Peripheral (MFP), 6850 ACIAs (keyboard and MIDI), YM2149 (sound chip), and 68000 CPU. Support chips which may cause the failure are specified by type and function (for example, 74LS244 buffer). Refer to the schematic to determine locator numbers.

Although it is not possible to account for all of the problems which can show up, this guide will indicate the solution in the majority of cases. If none of the recommended repairs fixes the problem, read the Theory of Operation section in the ST Field Service Manual to get an understanding of how the system works, or consult Atari Technical Support.

STARTUP SEQUENCE

System RAM errors. These errors are fatal--testing cannot proceed (but the test will repeat) because no RAM is available for program use. There is no display. Errors are printed to the RS232 port. Display failure address (Hex) and data written and read (binary). Data is displayed in binary to give a direct correspondence between the error and the chip which failed. The error occurred where the data written does not match the data read. For example, if data written = 0000000100000000 and data read = 0000000000001000, then the fourth and ninth bits failed, which correspond to U24 and U32 on a 520 ST. Likewise, data written = 1111111111111111 and data read = 1111111111111011 indicates bit 2 failed. Incorrect decoding of addresses at the Memory Controller can also cause RAM errors. This is detected in the disturbance and address tests.

I1 RAM/data line error—a 1 is walked across 16 bits of data, then 0 is walked across the data bus. Detects shorts and opens, Memory Controller, and buffer failures. Displays the address where the error was detected, the data written, and the data read back. Probable cause is defective RAM chip.

I2 RAM disturbance--fills low 2k with 0 and writes to all other locations up to 256k, then verifies low memory not affected. Detects RAM and Memory Controller failures. Displays address, data written, and data read.

I3 RAM address check—ascending and descending patterns are written to check for unique addressing. Detects RAM and Memory Controller failures. Displays address, data written, and data read.

I4 Memory configuration error. The memory controller did not respond with DTACK to a valid address. Bad Memory Controller or Glue.

I5 RAM sizing error. The test determined what type of RAM chips are in use and configured the memory management unit for the correct amount of RAM, but that amount of RAM was not found. Probable bad Memory Controller, possible bad RAM chip.

K0 Stuck key. A reset command was sent to the keyboard; the keyboard self-test detected a key pressed (no key should be depressed on power-up).

Check that the keys can move freely; replace keyboard.

K1 Keyboard status. A reset command was sent to the keyboard. The keyboard should perform a self-test and respond within 300ms with a status byte.

Replace keyboard, or 6850, or Glue. Verify (with oscilloscope) the signals between 6850 and keyboard. TXDATA (pin 6) should output data

immediately after power is turned on at computer; RXDATA (pin 2) should receive data from keyboard shortly after power-on and every time a key is pressed.

68000 or System Errors--may occur at ramdom times. Indicate failures in key system components.

E6 Autovector error--Internal 68000 instruction. IPL0 line may be floating or 68000 chip is bad.

E7 Spurious Interrupt--BUS ERROR was asserted during interrupt acknowledge cycle, indicating DTACK or VPA are not occuring within required time period. Replace Glue, Memory Controller, or 68901 (that order).

E8 Exception error--Processor executed instruction (not present in program) which caused exception processing. Either the processor is fetching bad instructions or the processor itself is bad.
Use oscilloscope to check for noisy data bus; locate source of noise if present (check clocks). If not, replace test cartridge or Glue or 68000.

E9 Instruction fetch error--the processor read data during an instruction fetch cycle which is not a legal instruction.
Follow steps under Exception error, above.

EA Address Error--the processor read an instruction which would cause it to access a word, long word, or instruction on an odd address. This error may indicate a programming bug as well as a hardware problem. If preceeded by another error, disregard this and fix the first error. Otherwise, it indicates the processor is not reading the correct data from the cartridge ROM.

Possible fixes are:
Replace test cartridge.
Replace Glue.
Replace 68000.
Examine data bus and clocks for excess noise; replace noisy part (compare against good system).

EB Bus Error--the processor addressed a device, but received no DTACK or VPA. This error will be followed by the address being accessed at the time of failure. Either the Glue chip is bad, or the address indicates the cause of failure.
Memory Controller: ff8001, ff8201-ff8209, ff8609-ff860d
Glue: ff820a
DMA Control: ff8604, ff8606
Video Shifter: ff8240-ff8260
Programmable Sound Generator: ff8800, ff8802
MFP: fffa01-fffa2f
6850 (keyboard): fffc00, fffc02
6850 (MIDI): fffc04, fffc06

Replace Glue or device being accessed. Sometimes the address displayed

will not be a legal device address. If the address is RAM (8—7ffff for 520k machine, 8—fffff for 1040k), it indicates the Memory Controller is not responding.

RAM TEST

The following errors display the failure address (Hex) and data written and read (binary). Data is displayed in binary to give a direct correspondence between the error and the chip which failed. The error occurred where the data written does not match the data read. For example, if data written = 0000000100000000 and data read = 0000000000001000, then the fourth and ninth bits failed, which correspond to U24 and U32 on a 520 ST. Likewise data written = 1111111111111111 and data read = 1111111111111011 indicates bit 2 failed. Incorrect decoding of address at the Memory Controller can also cause RAM errors.

10 RAM—Fatal error (low memory).

11 RAM--device error. RAM will not retain data written.

12 RAM--addressing error. Writes pattern (repeating every 64k) through memory to detect non-unique addressing.

13 RAM—64k block addressing. Extension of address test (which detects duplication within 64k boundaries), this tests for uniqueness of 64k block addresses.

Repair: for RAM test errors 10-12, replace Memory Controller; if symptom persists, replace the RAM chips indicated by the bits which failed (and restore the original Memory Controller). Error 13 may be caused by address lines A18-A21 not functioning. (Other address lines are tested in the start-up sequence.) These address lines are used by the following machines:

A21	4 MByte
A20	4, 2 MByte
A19	4, 2, 1 MByte
A18	4, 2, 1 MByte, 512k

If testing a 512k machine and error 13 appears, verify address 18 only; likewise, if testing a 1MByte machine verify A18 and A19, etc.; then replace Memory Controller or RAM if necessary.

All other control and bus lines for memory are tested in the start-up sequence; therefore, errors 10-13 will be due mostly to bad RAM and Memory Controller parts, with RAM chips causing the majority of failures.

ROM TEST

This test checksums the 16k and compares with the Boot ROM values. If both Boot ROMs compare, the screen turns green and "Boot ROMs OK" is

printed. If only one compares, the test fails. If both do not compare, 192k is checksummed and compared to the TOS ROM checksums. All six checksum are displayed with OK printed after each if it compares. If any does not compare, OK is not displayed and the screen turns red.

COLOR TEST

Note: there is a line along the right margin where the color is offset by one scan line. This is not a fault in the hardware. This is caused by the software changing the border color in the middle of the line.

The colors displayed are the three primary colors (red, green, blue), three secondary colors (cyan=green+blue, magenta=red+blue, yellow=red+green), and white (=red+green+blue). Each color is displayed at 8 levels of intensity. The source of these colors is the Video Shifter.

The Video Shifter has three outputs for red (R0, R1, R2), green (G0, G1, G2), and blue (B0, B1, B2). Each of these triples forms a counter which gives 8 levels of intensity for that color, depending on which of the outputs are on. Eight levels of red look like this:

The three outputs are then summed by a resistor network, and the sum of the current through the three resistors determines the voltage present at the input of the video driver. The value of the resistor at R0 is twice that of the resistor at R1, which is twice R2. This weighting allows us to get eight equal steps. The signal above will look like a staircase at the summing end:

The signal then passes through a transistor amplifier, and from there to the video monitor connector.

Symptoms and fixes:

1. Missing primary color--check the output of the transistor amplifier. Q3 is blue, Q4 is green, Q5 is red. Look for the staircase pattern. If signal is there, trace forward to the video connector, if not, trace backward to the Video Shifter, until the faulty component is found.
2. Primary colors present, secondaries missing or incorrect--replace Video Shifter.
3. Coarse change in intensity (not a smooth dark to light transition--replace Video Shifter or look for short on output.
4. Specks or lines on screen--this may be caused by bad RAM;

if RAM has been tested and is good, replace Video Shifter.

5. Wavering display, horizontal not syncing on the same line every time--the processor may be getting extra interrupts (if the processor is required to handle additional interrupts, it will not have time to change all 16 color registers during a horizontal scan). Examine the MFP interrupt request (pin 32). There should be an interrupt every 126 microseconds (2 display lines) from Display Enable (pin 20). If additional interrupts occur, find the source: the inputs at pins 22-29 should all be high.
NOTE: if the keyboard is not connected, the input to the 6850 will be low, causing continual interrupts. If no external (to the MFP) source for the interrupts is found, replace the MFP.

KEYBOARD TEST

On selecting the keyboard test, the self test is performed first, which, if passed, indicates the keyboard processor is working and communicating with the CPU, and no keys are stuck. If this test fails, no further testing can be performed. Assuming the self test passes (it takes less than 1/2 second) and this is the only test selected, the monitor will display the full keyboard, with the cursor keys and keypad keys below the normal typewriter keys. The operator can press any key and observe that the correct key on the screen changes (inverts color). Pressing the ESC key will exit the test. If more than one test has been selected, or multiple cycles of the keyboard test, only the self test will be performed.

ERRORS

K0 Stuck key—a key closure was detected while the keyboard self test was executing. (The program waits for the RETURN key release when the operator selects the test before starting testing.)

K1 Keyboard not responding—a command was sent to the keyboard processor and no status was returned witin the allowed time. Check communication through the 6850. The easiest way to do this is to observe the keycodes coming from the keyboard on pin 2 of the 6850 with an oscilloscope while pressing any key. If nothing is coming across, check the connection, replace keyboard if necessary. If data is getting to the 6850, verify that the interrupt (pin 7) is occuring and being cleared. Verify also that the interrupt at the MFP (pin 32) is happening and being cleared. If the 6850 has data coming in and no interrupt, replace it. If the MFP has an interrupt request (pin 26) and no interrupt (pin 32) replace it. If no problems are observed in the receiving circuit, select multiple cycles of the keyboard test and verify that the 6850 is sending the command to the keyboard. If not, replace the 6850.

K2 Keyboard status error--the self test command was sent to the keyboard, upon completion of the test, the keyboard sent and error status. Replace the keyboard.

MIDI TEST

This test requires that the MIDI loopback connector be installed. The operator should verify that the LED on the connector blinks, as this tests the MIDI "through" output (pin 3 on the MIDI OUT connector).

ERRORS

M0 Data not received—trace the data signal from the 6850 pin 6 to the 6850 pin 2. If the signal does not arrive, replace the defective component. If the data does arrive, verify that the interrupt occurs at the 6850 and at the MFP.

M1 Write/Read data mismatch--data written was not the same as data read. Compare outgoing and incoming data. Replace the 6850 or driver or receiver.

M2 Input frame error--bad 6850 or noisy signal because of bad driver or receiver.

M3 Input parity error—bad 6850 or noisy signal because of bad driver or recevier.

M4 Input data overrun—the 6850 received a second byte before the first was read by the CPU. Probable bad 6850, but check the incoming data (pin 2) with the outgoing data (pin 6) to make sure spurious bytes are not being generated by bad drivers. Also can be caused by the MFP not reponding to the interrupt.

LED not blinking: check output of 74LS04 pin 4 and 74LS05 pin 8.

RS232 TEST

This test requires that the RS232 loopback connector be installed. If a terminal has been installed at the RS232 port, the message "no loopback connector" will be displayed at the terminal. The monitor screen will display several error messages.

As this test does not simulate the worst case loading of an RS232 line, it may be that the test will pass, but the port will not work in a particular application (for example, driving a very long cable). In this case replacing the 1488 driver and 1489 receiver should correct the problem.

This tests initially without interrupts at 9600 bits/second (bps), then at 300, 600, 1200,...19200 bps, displaying the rate if there is an error, then tests the interrupts at 9600 bps.

ERRORS

Test data ttransmission--function of MFP (68901)
Examine SO/SI signal at driver and receiver. If clean or missing, replace MFP; if noisy, replace driver or receiver.

S0 Data not received—no data detected by receiver.

S1 Data mismatch--data read did not match data written.

S2 Input frame error--incorrect time between start and stop bits.

S3 Input parity error—input data had incorrect parity.

S4 Input data overrun—a second byte was received before the byte in the receiver buffer was read by the CPU.

S5 No IRQ—replace MFP.

S6 Transmit error (68901)—the 68901 transmitter failed.

S7 Transmit error interrupt--an error condition was created to generate an interrupt, and the MFP did not respond.

S8 Receive error interrupt--an error condition was created to generate and interrupt, and the MFP did not respond.

Test protocol signals--outputs of YM2149, inputs of MFP, and 1488, 1489 drivers:

S9 RI - DTR not connected
Trace signal from DTR (YM2149 pin 17) to RI (MFP pin 28).
Replace YM2149, 1488, 1489, or MFP as needed.

SA DCD - DTR not connected
Trace signal from DTR (YM2149 pin 17) to DCD (MFP pin 23).
Replace YM2149, 1488, 1489, or MFP as needed.

SB RTS - CTS not connected
Trace signal from RTS (YM2149 pin 18) to CTS (MFP pin 24).
Replace YM2149, 1488, 1489, or MFP as needed.

TIMING TEST

Tests MFP timers, Glue video timing, and Memory Controller video addressing.

T0 MFP timer error. The 68901 Multi-Function Peripheral chip timer(s) did not generate an interrupt in the correct time period.

Replace MFP or Glue.

T1 Vertical Sync—Glue is not generating vertical blank in the

required time period.

Replace Glue.

T2 Horizontal Sync—Glue is not generating horizontal blank in the required time period.

Replace Glue.

T3 Display Enable—the 68901 is not generating an interrupt or Glue is not generating the DE output.

Replace Glue or 68901.

T4 Video Counter Error, Memory Controller—the Memory Controller is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes.

Replace Memory Controller.

DMA PORT TEST

Tests high speed data transfer between the RAM of the unit under test and the test fixture RAM, via the DMA controller.

D0 DMA timed-out—no DMA occurred, or the HDINT interrupt was not processed by the MFP. Verify the DMA Controller responds to HDRQ (pin 23 low to high) from the test fixture with ACK (pin 37 high to low) at a 1 MHz rate. Verify that HDINT occurs at the MFP and the MFP responds with INTR (pin 32 high to low). Replace DMA Controller or MFP.

D1 DMA counter error—the number of bytes transferred was incorrect (not a multiple of 512). Replace the Memory Controller or the DMA Controller.

D2 Data mismatch error—the data read in from the DMA port was not the same as the data written out the port. Replace the DMA Controller. If problem persists, verify the data lines to the port connector for opens, shorts, or possible loading by the 1772.

D3 DMA status error--the DMA Controller was unable to respond to a request for data transfer. Replace the DMA Controller or Glue.

MONOCHROME MONITOR -

This test verifies the interrupt channel for the monochrome monitor and displays a test pattern to check the monochrome video. After selecting the test, the RGB monitor will display "CONNECT MONOCHROME MONITOR". When the monochrome monitor is connected, it

will display a crosshatch pattern. Each vertical and horizontal line is two pixels wide. The test is meant to confirm that all pixels are displayed in high resolution mode.

Symptoms and fixes

No picture on monochrome:
Check MONO output on Video Shifter (pin 30).
1. If it is always low, check MFP pin 29.
a. If MFP pin 29 is low, repeat the test, looking for an interrupt request (high to low on MFP pin 32) when the monochrome monitor is connected.
1) If this does not occur, replace the MFP.
2) If it does occur, replace the Video Shifter.
b. If MFP pin 29 is high, the monochrome connector is not making contact, or the trace is open.
2. If Video Shifter pin 30 has a signal, trace out to the connector. Replace the transistor or find the open or short.

Picture broken up:
Replace Video Shifter.

Picture wavering, distorted:
The monochrome monitor can be affected by a nearby color monitor. Turn off the color monitor.

FLOPPY DISK CONTROLLER TEST

Either one or two disk drives may be tested, and they may be single or double sided. The diskettes must not be write protected. The operator should install the drives by selecting the "I" option from the main menu, then typing "1" for single sided, "2" for double sided, or nothing for no disk when prompted. If the drives are not installed when the test is selected, the test program will automatically attempt to determine how many and what type of disks are connected by formatting, writing, and reading track 79 of both sides of both disks. When this is determined, the disks are installed for future reference (they will appear on the main menu when the test is over) and testing will proceed.

This tests function of 1772 disk controller, drivers, YM2149, MFP, and DMA chips. DMA and Printer ports should be tested first to eliminate those parts as possible reasons for failure. The 1772 and the drivers are the primary components to suspect in case of failure; however, the MFP and DMA Controller may also cause problems. The media and disks must be known to be good. The operator should have back-up disks available or be sure they are good before replacing components on the 520 ST.

ERRORS

No floppies connected—the cable is not connected properly or there is no power to the drive.

F0 Drive A (or B) not selected—drive was installed, but attemping restore (seek to track 0) failed. Check connection of cables, power to drive. Verify the light on the front of the drive goes on. Listen for the sound of the head seeking (the slide on the diskette should open). If all this is happening, see if TR0 (pin 23) on the 1772 is going low. If so, check for an interrupt on pin 28 of the 1772. If none, replace the 1772. Else trace the interrupt to the MFP, verify that the MFP responds by asserting INTR (pin 32).

If the drive is not being selected (no light), check the YM2149 chip. Pin 20 should go low when drive A is selected, pin 19 should go low when drive B is selected. If not, replace the YM2149.

F1 Format error—error occured during format of disk. A more specific error message should follow.

F2 Write error—error occured while writing the disk. The specific error messager should follow.

F3 Read error—verify the diskette. Replace the 1772.

F4 Seek error—examine STEP, MO, DIRC outputs from the 1772, and verify they are transmitted by the 74LS05 driver. If the driver looks OK, replace the 1772.

F5 Write protected—Check write protect tab. It should be pushed towards outer corner (on some diskettes this opens a see-through window). Verify that the WP line (1772 pin 25) is going low during the test; if it is and this error occurs, replace the 1772; if not the problem is with the disk drive.

F6 Read compare error—data read from disk was altered from what was written. Replace DMA Controller, if still bad, replace 1772.

F7 DMA error—error in transfer of data between 1772 and memory. Replace DMA Controller; if still bad, check FDRQ (DMA Controller pin 21 and 1772 pin 27); it should normally be low and go high with each data byte transferred. If stuck high, try pushing the reset button and verify that MR (1772 pin 13) goes low. If not, trace RESET. If FDRQ is still stuck, replace the 1772.

F8 DMA count error—replace the Memory Controller, if not fixed, replace the DMA Controller.

F9 CRC error—verify the disk drive and diskette (test with known good unit). Replace the 1772.

FA Record not found—verify the disk drive and diskette.
Replace the 1772.

FB Lost data--data is not being read from the 1772 as fast as it is being read in from the disk. There is a failure in the DMA controller or Glue chip.

FC Side select error--single sided drive--YM2149 side select line failed, or single sided drive is installed as a double sided drive. Verify that SS0 (YM2149 pin 21) is switching. If not, replace YM2149. Verify that SS0 goes to J3 pin 2.

PRINTER AND JOYSTICK PORTS TEST

For purposes of testing, the printer port and joystick ports are logically connected. A failure of one may affect the other.

P0 Printer port error--writes data to port, latches data on test fixture, reads data from port. Walks 1 across 8 bits. Verify that the data lines (pins 6-13) and strobe (pin 16) are toggling when test is run. If not, and the RS232 test fails with RI-DTR, DCD-DTR, and RTS-CTS, the YM2149 chip is probably not being selected: verify chip selects and 2MHz clock, or replace Glue. If the YM2149 is selected and is not outputting signals, replace the chip. Also verify that J11 (Joystick 0) pin 3 is pulled up.
If none of the above fixes it, the test fixture may be bad.

P1 Busy line error--the input to the MFP is not being read, or STROBE output from the YM2149 is not functioning, or Joystick 0 pin 3 is not connected. If the Busy line error also occurs, replace YM2149. Otherwise, replace the MFP. If this does not fix the problem, there is probably a broken trace. See if the signal arrives at MFP pin 22 from J5 pin 11. If there is no signal, the test fixture may be bad.

J0 Joystick Port 0--this keyboard input not functioning. If the Busy line error occurs, fix that first. Otherwise replace the keyboard. Check continuity from J11 pins 1,2,3,4 to J12 pins 12,10,9,8.

J1 Joystick Port 1--this keyboard input not functioning. If the Busy line error occurs, fix that first. Otherwise replace the keyboard. Check continuity from J10 pins 1,2,3,4 to J12 pins 7,5,4,3.

J2 Joystick time-out--joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU the same way keystrokes are sent. This error can be caused by printer port failure (should be detected by printer port error), keyboard failure (should be detected at power-up by keyboard self test) or failure in the test fixture.

J3 Left button line error--this input to the keyboard is not functioning. If the Busy line error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, check continuity from J10 pin 6 to J12 pin 11.

J4 Right button line error--this input to the keyboard is not functioning. If the Busy line error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, check continuity from J11 pin 6 to

ST COMPUTER MANUFACTURING TEST
REVISION 4.0 B1 4.0C 6/27

TEST EQUIPMENT

The following equipment will be needed to test the ST computer:

* Atari SC1224 RGB Monitor (or similar)
* Atari SM124 Monochrome Monitor (or similar)
* Atari SF314 Floppy Disk Drive
  (520ST requires two SF314.)

* ST Port Test Fixture
* RS232 Loop-Back Connector
* MIDI Loop-Back Cable
* ST Manufacturing Test Cartridge
* Diskettes
* Expansion Connector test fixture (MEGA ST only)

Optional (for troubleshooting):
* RS232 terminal (or ST with VT52 emulator)

TEST CONFIGURATION

With the power switch off, install the test cartridge (IMPORTANT--if the cartridge does not have the plastic enclosure, BE SURE THE CARTRIDGE IS INSTALLED WITH THE CHIPS FACING DOWN). Connect cables from test fixture into the hard disk port, parallel port, and joystick/mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the RS232 and MIDI loopback connectors into their ports. Plug the color monitor into the monitor output (a monochrome can be used instead). Drawing number C026110 shows the test hook-up. The expansion test fixture plugs into the expansion connector and expansion power plug.

Power on the unit. Some tests will be run automatically; in a few seconds the menu screen should appear. If the screen does not appears, set aside the unit for repair.

Power-up

The diagnostic program performs several tests on power-up. In particular, the messages "Recovering from Bus Error" and "Testing MFP, Glue timing, Video" will appear, and the screen will appear scrambled for a few seconds before the menu is printed. The screen will turn red (dark background in monochrome) if an error occurs in the initial testing, with a message indicating the failure. The lowest 2 Kbytes of RAM is tested on power-up; if a location fails, the error will be printed to the RS232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there is no stack or system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen

may turn red). Repair RAM.

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS232 port. The diagnostic program looks for keystrokes from the RS232 device. If the display is unreadable, the RS232 terminal should be used for troubleshooting. All messages are printed to the RS232 port as well as the screen.

RAM initialization errors (visible on RS232 device only).
Errors I1-I3 will display the data written, data read, and address:

I1--error in RAM or data bus. Walking 1 or 0 across the data bus.
I2--RAM disturbance error. Write to one location alters another location.
I3--RAM addressing error. Tested using pattern to show up address problems, as well as bad cells.
I4--Memory configuration error. The Memory Controller is not responding correctly.
I5--RAM sizing error. Topmost address for this configuration is bad. Second bank is not selected or bad RAM cell at this address.
I6--Servicing bus error. On start-up, this message is printed, then a bus error is created. If the processor halts while attempting to service the bus error, the message will remain on screen. Otherwise, the message is cleared when the menu screen is printed.
I7--Bus error not serviced. This error is reported if the bus error was not detected.

Other initialization errors may be found under descriptions for the RAM test (R errors), the keyboard test (K errors), and timing tests (T errors).

Test Menu

The normal screen will be dark blue with white letters. The test title and revision number are displayed at the top, with the amount of RAM and keyboard controller revision below, and a test menu below that. To select tests, the user types the key corresponding to that test.

Menu Example:

```
                    ST Computer Manufacturing Test Rev. 4.0 B
                       c 1987, Atari Corp.
      RAM              Keyboard revision 2          60 Hz

   0  Auto test: 1--/
   1  RAM Test          2  O.S. ROMs          3  Color
   4  Keyboard          5  MIDI               6  Serial Port
   7  Audio             8  Timing             9  DMA Port
   (  Printer/Joystick Ports                   )  Floppy Disk
   /  High resolution monitor
   *  Blitter           +  Expansion

   E  Examine/Modify memory
   B  Set RS232 rate
   V  Toggle video output--50/60 Hz
```

Note that the amount of RAM and the keyboard revision are variable.

Selection 'E' enables the operator to examine or modify RAM or hardware registers. 'B' enables the operator to change the baud rate on the RS232 port. Pressing the up arrow increases it, pressing the down arrow decreases it. 'V' switches the vertical scan rate between 50 and 60 Hz (color only).

Note: Test items applied to each model of ST computers are as follows.

		ST Computers			
No.	Test Item	520ST	520STF(M)	1040STF(M)	MEGA ST
1.	RAM Test	o	o	o	o
2.	O.S. ROM's	o	o	o	o
3.	Color	o	o	o	o
4.	Keyboard	o	o	o	o
5.	MIDI	o	o	o	o
6.	Serial Port	o	o	o	o
7.	Audio	o	o	o	o
8.	Timing	o	o	o	o
9.	DMA Port	o	o	o	o
10.	Printer / Joystick Ports	o	o	o	o
11.	Floppy Disk	o	o	o	o
12.	High Resolution Monitor	o	o	o	o
13.	Blitter	-	-	-	o
14.	Expansion	-	-	-	o

Summary of Tests

AUTO TEST

This selection runs a sequence of 0 (RAM) through / (high resolution). As each test completes, the next test will automatically be started when the space bar or Enter key is pressed.

RAM TEST

RAM is tested in three stages: low 2 kbytes, middle (up to 64k), and from 64k to top. The test patterns used are: all 1s, all 0s, a counting pattern (data=low word of the address), reverse counting pattern (data=complement of address low word). The counting pattern is copied from the top and bottom of a 32 Kbyte buffer into the current 32 Kbytes of video RAM, then shifts video RAM to a new area, verifies the pattern, and repeats the test, until the top of RAM is reached. Finally, addressing at 64k boundaries is checked by writing unique pattern in last 256 bytes of each 64k block.

If an error occurs, the error code is displayed, followed by the address, data written, data read, and the bits which did not agree. E.g.: " R2 45603E W:603E R:613C bad bits: 1,8".

In units having more than one bank (i.e., 1040ST, 4160ST) the address as well as the bit position must be used to find the correct chip. The following table gives a correspondence between the addresses and banks for various models:

	520	1040	2080	4160
0-7ffff	bank 0	bank 0	bank 0	bank 0
80000-fffff		bank 1	bank 0	bank 0
100000-1fffff			bank 0	bank 0
200000-3fffff				bank 1

(A bank is a 16 bit wide group of RAMs. A bank may consist of 256k bit chips--256k x 16 = 4 Mbit or 512k bytes--or 1Mbit chips--1Mbit x 16 = 16 Mbit or 2 Mbytes.)

RAM ERROR CODES

Except where noted, repair by replacing the RAM chip corresponding to the indicated bit(s).

R0--low memory failed while setting up to run test.
R1--failed walking 1s or 0s.
R2--failed address (counting pattern).
R3--failed 64k boundary test. Probable failure in Memory Controller.
R4--failed while displaying area tested (video RAM).

ROM TEST

This test reads all bytes from operating system ROMs and calculates the checksums. It compares against known values of checksums and determines if good or bad. It checks known values for U.S./Canada, United Kingdom, French, German, and Spanish (PAL and NTSC) ROMs.

For each ROM the checksum and type is displayed. The test fails if any unknown checksums are found or if the ROMs are not all of the same type (e.g. mixed French and German). Incorrect checksums are indicated by an arrow. If a ROM is found in the wrong position, the test fails. The out-of-place ROM is indicated by an arrow.

New revisions of TOS will cause this test to fail if not incorporated into the current version of the diagnostic. If you receive TOS revisions before receiving the diagnostic revision, it will be

necessary to verify the checksums yourself.

COLOR TEST

This test verifies the Video Shifter. Seven color bands are displayed: red, green, blue, cyan, magenta, yellow, and white. Each band consists of 8 levels of intensity. All 16 color palettes are represented, each palette is a vertical strip across the screen (strips should not be discernable, but each color should be a straight line across the screen). Because of the tight timing involved, keystroke interrupts will cause the display to jitter.

The operator should see that there are no gaps or missing scan lines in the display. If lines are missing, check the three outputs on the Video Shifter for that color, and verify the values of the resistors on the output. Too low a brightness setting on the monitor will cause the monitor not to distinguish between fine levels, making it appear there are only four levels being output.

The Video Shifter has three outputs for red (R0,R1,R2), green (G0,G1,G2) and blue (B0,B1,B2). Each of these triples is summed together by a resistor network to give 8 levels of intensity for each color, depending on which of the outputs are on. The values of the resistors give different weight to each output. The value of the resistor at R0 is twice that of R1, which is twice that of R2. This allows us to get 8 equal steps on the summed outputs. For example, R0 on and R1 and R2 off = 1/8, R0 off, R1 and R2 on = 7/8. This signal then passes through a transistor amplifier, and from there to the video monitor connector.

Symptoms and fixes:

1. Missing primary color. Check the output of the transistor amplifier. Q3 is blue, Q4 is green, Q5 is red. Look for a staircase pattern (eight levels of intensisty). If the signal is there, trace forward to the video connector, if not, trace backward to the Video Shifter, until the faulty component is found.
2. Primary colors present, secondaries missing or incorrect. Replace the Video Shifter.
3. Coarse change in intensity (not a smooth dark to light transition). Replace Video Shifter or look for a short on the output of one of the three color outputs for the appropriate color.
4. Specks or lines on the screen. This can be caused by bad RAM; if RAM has been tested and is good, replace the Video Shifter.
5. Wavering display, horizontal lines not occuring in the same place every time. The processor may be getting extra interrupts (if the processor is required to handle additional interrupts, it will not have timer to change all 16 color registers during a horizontal scan time). Examine the MFP interrupt request (pin 32). There should be an interrupt every 126 microseconds (2 display lines) from Display Enable (pin 20). If additional interrupts occur, locate the source: the inputs at pins 22-29 should all be high. If no external (to the MFP) source for the interrupts is found, replace the MFP.

NOTE: if the keyboard is not connected, the input to the 6850 will be low, causing continual interrupts.

KEYBOARD TEST

Two types of test are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. The operator presses 15 keys (highlighted), representing the rows and columns of the keyboard matrix, and observes that the corresponding character on the screen changes (reverses background color). If any other keystrokes are detected, the test fails. Once all 15 keys are detected, the test passes. At this point, any key may be pressed without causing the test to fail. The test is exited by pressing the escape key.

The self-test checks communication between the CPU and the keyboard microcomputer, and checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

KEYBOARD ERROR CODES

K0--Stuck key. A key closure was detected while the keyboard self test was executing.

K1--Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time. The keyboard needs to be replaced or the communication channel through the 6850 is not functional.

K2--Keyboard status error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status. Replace the keyboard.

MIDI TESTS

This test sends data out the MIDI port, (data loops back through the cable) and reads from the input and verifies the data is correct. This also tests the interrupt from the 6850 through the MFP chip. The LED in the loopback cable will blink as data is sent (not all cables have the LED).

MIDI ERROR CODES

M0--Data not received. Trace the signal from the output of the 6850, through the drivers, loopback cable, and receivers to the input of the 6850. Replace the defective component.

M1--Write/Read data mismatch. The data written was not the same as the data read. Replace 6850.

M2--Input frame error. Bad 6850 or bad driver or receiver causing noisy signal.

M3--Input parity error. Bad 6850 or bad driver or receiver causing noisy signal.

M4--Input data overrun. The 6850 recevied a byte before the previous byte was read. Probable bad 6850, also can be caused by the MFP not reponding to the interrupt request.

RS232 TESTS

First the RS232 control lines are tested (which are tied together by the loopback connector), then the data loopback is tested. Data is checked transmissing/receiving using a polling method first, then using interrupts.

If these tests pass, the screen will turn yellow and display the message "Open loopback circuit and press any key". The loops between send/receive, RI/DTR, DCD/DTR, and CTS/RTS should be opened at this point and a key pressed. The test then verifies that these signals are not shorted together.

Data is transmitted at 300, 600, 1200...19200 bps. Data transmission is performed by the MFP and the 1488 and transmission is performed by the MFP and the 1488 and 1489 driver and receiver chips. Interrupts are a function of the MFP. Control lines are output by the PSG chip and input on the MFP.

RS232 ERROR CODES

Data transmission error:

S0--Data not received. Check signal path: MFP pin 8 to J6 pin 2 via 1488 to J6 pin 3 to MFP pin 9 via 1489.

S1--Data mismatch. Data read was not what was sent. Check integrity of the signal. May be bad driver, receiver, or MFP.

S2--Input frame error. Incorrect time between start and stop bits. Probable MFP failure.

S3--Input parity error. Input data had incorrect parity. Probable MFP failure.

S4--Input data overrun. A byte was received before the CPU read the previous byte. MFP failure or, less likely, Glue failure.

S5--No IRQ. CPU did not detect an interrupt by the MFP. MFP or Glue failure.

S6--Transmit error. MFP transmitter failed.

S7--Transmit error interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.

S8--Receive error interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.

S9--RI/DTR connection. Signal sent at DTR is not detected at RI.

S10--DCD/DTR connection. Signal sent at DTR is not detected at DCD.

S11--RTS/CTS connection. Signal sent at RTS is not detected at CTS.

S12--RI shorted to DTR.

S13--DCD shorted to DTR.

S14--RTS shorted to CTS.

S15--SD shorted to RD.

AUDIO TEST

Outputs a low to high sweep on each of the three sound channels. One cycle of each channel is performed. If a channel is missing, replace the PSG chip. If no sound is heard, verify the output of the chip with an oscilloscope, and trace the signal to the monitor output connector. If no output from the PSG, verify the PSG is being selected by running the printer port or RS232 test (these tests both select the PSG).

TIMING TESTS

These tests are run at power-up as well as being selectable from the menu. The MFP timers, the Glue timing for VSYNC and HSYNC, and the Memory Controller video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as

this test is run. There are two tests which check the bus timing for the 1772 and PSG chips. An error message is printed to the screen, then the test is run. If the test passes, the message is erased. If not, a Bus Error will occur and the message will remain. If a terminal is connected to the RS232 port, the message will not be erased, but "Pass" will be printed.

TIMING TEST ERROR CODES

T0--MFP timer error. One or more of the four timers in the MFP did not generate an interrupt on counting down .

T1--Vertical Sync. Glue is not generating vertical sync in the required time period.

T2--Horizontal Sync. Glue is not generating horizontal sync in the required time period.

T3--Display Enable. Glue is not generating DE output or the MFP is not generating an interrupt.

T4--Video Counter Error. The memory controller is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes.

T5--PSG Bus Error. The PSG chip is defective.

T6--1772 Bus Error. The 1772 chip is defective.

DMA TESTS

Four sectors (2048 bytes) of data are written to the RAM on the port test fixture via high speed DMA, then read back and verified. This test is repeated many times for RAM addresses throughout the range of RAM.

DMA TEST ERROR CODES

D0--DMA timed out. No DMA occurred due to faulty DMA Controller, Glue, or Memory Controller, or the HDINT interrupt was not processed by the MFP. The failure can be isolated by seeing if the DMA Controller responds to HDRQ from the test fixture with ACK. Verify the MFP by seeing that the HDINT input causes an INTR output from the MFP.

D1--DMA counter error. the number of bytes transferred was incorrect. The Memory Controller or DMA Controller is bad.

D2--Data mismatch error. The data received from the DMA port was not the same as the data sent. Replace the DMA Controller. If the problem persists, check the data lines to the port for opens and shorts. A third possibility is that a defective 1772 is loading the bus.

FLOPPY DISK TESTS

Select 1 or 2 key depending on ST product to be tested.

Key " 1 " - 520STF(M)

Key " 2 " - 520ST, 1040STF(M), MEGA ST

1. Format side 0 of drive A.
2. Write tracks 0, 1, 2, 79, 0; read same.
3. Format side 1, track 0; read same. (Only when key " 2 " is selected.)
4. Format drive B, side 0; track 0; write and read same.
5. Format side 1, track 0; read same.
6. Read disk A, side 0, track 0.
7. Prompt user to insert write protected disk, then attempt to write the disk and verify that the status is write protected.

FLOPPY TEST ERROR CODES

F0--Drive not selected. Failed attempting restore (seek to track 0). Check connection of cables, power to drive. F1--Drive select error. Not differentiating between drive A and drive B.

F2--Data compare error. Data read back from the drive was not what was written.

F3--Not write protected. The drive or controller did not return write protect status when attempting to write a protected diskette.

F4--Seek error. Verify that the STEP, MO, and DIRC outputs from the 1772 are sent to the drive. Probable failure in the 1772, but the drive is also suspect.

F5--Write protected. Check the write protect tab on the diskette. If OK, verify that the WP input (1772 pin 25) is going low during the test; if it is, then the 1772 is defective; if not, the problem is with the disk drive.

F6--Read compare error. Data read from the disk was not what was supposed to be written. Check in the following order: diskette, disk drive, 1772, and DMA Controller.

F7--DMA error. DMA Controller could not respond to a request for DMA. Replace the DMA Controller. If error persists, check FDRQ while running the test. It should normally be low and go high with each data byte transferred. If stuck high, push the reset button and verify that MR (1772 pin 13) goes low. If not, trace RESET to its source. If MR is OK, but FDRQ is still stuck, replace the 1772.

F8--DMA count error. Replace the Memory Controller, if that does not fix it, replace the DMA Controller.

F9--CRC error. The diskette or disk drive may be bad, else replace the 1772.

F10--Record not found. The 1772 could not read a sector header. May be a bad diskette, drive or 1772. If the test fails drive A but not drive B, the 1772 is not at fault (likewise fails B not A).

F11--Lost data. Data was transferred to the 1772 faster than the 1772 could transfer to the DMA Controller. If DMA Port test passes, the 1772 is probably bad. The DMA Controller could also be at fault.

F12--Side select error--single sided drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.

F13--Drive not ready. The format/write/read operation timed-out. Probably a bad disk drive. Verify by checking another drive. Could also be a faulty 1772.

PRINTER AND JOYSTICK PORT TESTS

The port test fixture is used to test the parallel printer port and joystick ports. The parallel port test writes to a latch on the test fixture and reads back data. The joystick port test outputs data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU.

PRINTER/JOYSTICK ERROR CODES

P0--Printer port error. Data read from the printer port was not what was written. Verify that the data lines on the PSG chip (pins 6-13) are toggling when the test is run. If not, run the RS232 test. If the RI-DTR and DCD-DTR errors occur, the chip is probably not being selected. Check if the chip selects are being activated and the 2MHz clock is present. If the PSG is selected and not outputting signals, replace it. If the data lines toggle, verify continuity. Also verify that J11 (Joystick 0) pin 3 is pulled up. Verify the test fixture is good by testing another computer. If it is OK, replace the PSG.

P1--Busy input error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected. If the P0 error also occurs, see handling for that. Otherwise, look for a signal arriving at MFP pin 22 from J5 pin 11. If no signal at J5, the test fixture may be bad. Verify with another computer. J0--Joystick Port 0. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 12,10,9,8 respectively.

J1--Joystick Port 1. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 7,5,4,3 respectively.

J2--Joystick time-out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, keyboard-CPU communication line, or a faulty test fixture. If the power-up keyboard test passes, this eliminates any problem with keyboard-CPU communication.

J3--Left button input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, also check continuity from J10 pin 6 to J12 pin 11.

J4--Right button input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, also check continuity from J10 pin 6 to J12 pin 6.

HIGH RESOLUTION MONITOR

If this test is selected while a color monitor is connected, a message is displayed to connect the monochrome monitor. The CPU waits for an interrupt from the MONOMON input to the MFP, and when received (the operator connects the monochrome monitor), changes the display to high resolution. The display screen shows horizontal and vertical lines, each 2 pixels in width. The screen will reverse every two seconds. When the operator sees the display is correct, he unplugs the monochrome monitor and re-connects the RGB monitor and the display should return to normal.

BLITTER

Test block transfer of data from one part of memory to another, using the blit chip. If no blit chip is installed or if there is no DTACK signal from the chip, the message "No blitter installed" will be displayed. If error B1 occurs, the faulty part may be the blitter or the MFP chip. In all other cases, the fault is almost certainly in the blitter, assuming the RAM test has passed.

B1--Blitter time-out. Operation complete was not detected (MFP I3 input, pin 25, is used for this signal).
B2--Halftone RAM. Bad RAM in the blit chip.
B3--Endmask. Bad logical masking function in blit chip.
B4--Operation. Bad logical operation in blit chip.
B5--Halftone op. Bad logical operation with halftone RAM in blit chip.
B6--Skew. Bad logical operation in blit chip.
B7--Reverse blt. Counters are not operating in high-to-low direction.
B8--Force extra source read.
B9--Smudge.
B10--X count.
B11--Y count.

EXPANSION and CLOCK

Test the real-time clock chip. First determine if the chip is there by writing into RAM (registers) and reading back. Then start the clock, wait one second, and verify that one second has ticked on the second counter.

Test all bus signals on the expansion connector. If no test fixture is installed, or if there is no DTACK signal from the test fixture, the message "No expansion test fixture" will be displayed.

Control lines BR, BG, BGACK, VMA, VPA, E, BERR, FC0, FC1, FC2, and HALT are verified by the LEDs on the test fixture. If the light is on after completing all tests, the line is open. BGACK will go out only after running the DMA or Floppy Disk tests.

C0--the real-time clock chip is not there, or not alive. We could not write into clock chip RAM.
C1--the clock chip is there, but not ticking off seconds.
EX0--bad bit. Walking 1 across the data bus revealed a bad data bit.
EX1--external RAM error, low byte. Low order address lines may be open on the expansion connector.
EX2--external RAM error, high byte. High order address lines may be open on the expansion connector.
EX3--INT3 error. INT3 line from the expansion connector is not being detected.
EX4--INT5 error. INT5 line from the expansion connector is not being detected.
EX5--INT7 error. INT7 line from the expansion connector is not being detected.

ERROR CODES QUICK REFERENCE

This is a brief summary of all error code which may occur when running the diagnostic.

INITIALIZATION (Errors occuring before the title and menu appear.)

I1 RAM data line is stuck.
I2 RAM disturbance. Location is altered by write to another location.
I3 RAM addressing. Wrong location is being addressed.
I4 MMU error. No DTACK after RAM access.
I5 RAM sizing error. Uppermost address fails.

EXCEPTION (may occur at any time)

E1--E5 not used
E6 Autovector error. IPL0 is grounded or 68000 is bad.
E7 Spurious interrupt. Bus error during exception processing. Device interrupted, but did not provide interrupt vector.
E8 Internal Exception (generated by 68000).
E9 Bad Instruction Fetch.
EA Address error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceeded by a bus error or bad instruction fetch.
EB Bus error. Generated internally by the 68000 or externally by Glue. Usually caused by device not responding. Displays the address of the device being accessed.

RAM

R0 Error in low memory, possibly affecting program execution.
R1 Error in RAM chip.
R2 Address error. Bad RAM chip or memory controller. Address line not working.
R3 Address error at 64k boundary.
R4 Error during video RAM test. Bad RAM chip.

KEYBOARD

K0 Stuck key
K1 Keyboard controller is not responding.
K2 Keyboard controller reports error.

MIDI

M0 Data not received.
M1 Data received is not what was sent.
M2 Data input framing error.
M3 Parity error.
M4 Data overrun. Byte was not read from the 6850 before next byte arrived.

SECTION SEVEN
PARTS LISTS AND ASSEMBLY DRAWINGS

PART NUMBER	DESCRIPTION	LOCATION
	CAP 10pF 50V 5% CH. CER AXIAL	C124
	CAP 22pF 50V 5% CH. CER AXIAL	C51
	CAP 12pF 50V 5% CH. CER AXIAL	C48
	CAP 30pF 50V 5% CH. CER AXIAL	C68,69
	CAP 33pF 50V 5% CH. CER AXIAL	C106,120
	CAP 68pF 50V 5% SL. CER AXIAL	C50
	CAP 100pF 50V 5% CH. CER AXIAL	C28,60~63
	CAP 150pF 50V 5% CH. CER AXIAL	C26
	CAP 680pF 50V 10% CH. CER AXIAL	C32,34
	CAP 1000pF 25V 20% X. CER AXIAL	C46,49
	CAP 4700pF 50V 20% X. CER AXIAL	C44
	CAP 0.01uF 50V 20% X. CER AXIAL	C3,4
	CAP 0.022uF 50V 30% X. CER AXIAL	C123
	CAP 0.1uF 25V Z. CER AXIAL	C1,2,5,6,10,11,13,15,24 C31,33,36,38,40,42,52,59 C64,67,70,72,119,121,122
	CAP 0.22uF 25V Z. CER AXIAL	C73~C104
	CAP 0.47uF 25V A. CER AXIAL	C39,45
	CAP 470pF 50V 10% B. CER AXIAL	C109~113,115~118
	CAP 47pF 50V 5% CH. CER AXIAL	C47,107
	CAP 4.7uF 25V ELEC. AXIAL	C25,27,30
	CAP 22uF 16V ELEC. AXIAL	C7,8
	CAP 47uF 16V ELEC. AXIAL	C9
	CAP 470uF 16V ELEC. AXIAL	C105
	CAP 22uF 16V ELEC. RADIAL	C71
	CAP 100uF 25V ELEC. RADIAL	C43
	CAP 470uF 16V ELEC. RADIAL	C35
	CAP 1uF 50V ELEC. AXIAL NPO	C12,14
	CAP 4.7uF 35V ELEC. AXIAL NPO	C29
	RES 1 OHM 1/4W 5% CARBON	R17
	RES 27 OHM 1/4W 5% CARBON	R27,28,34,58,101
	RES 33 OHM 1/4W 5% CARBON	R68,76
	RES 47 OHM 1/4W 5% CARBON	R63,67
	RES 68 OHM 1/4W 5% CARBON	R90,91,93,94
	RES 100 OHM 1/4W 5% CARBON	R24,31,35,50,59,103,105
	RES 150 OHM 1/4W 5% CARBON	R51,52
	RES 220 OHM 1/4W 5% CARBON	R1~5,15,62,104
	RES 470 OHM 1/4W 5% CARBON	R102
	RES 560 OHM 1/4W 5% CARBON	R55
	RES 820 OHM 1/4W 5% CARBON	R12
	RES 1K OHM 1/4W 5% CARBON	R11,16,21~23,60,61 R64~66,77,82~87
	RES 1.2K OHM 1/4W 5% CARBON	R18,20
	RES 1.5K OHM 1/4W 5% CARBON	R106
	RES 2.4K OHM 1/4W 5% CARBON	R45~47
	RES 3K OHM 1/4W 5% CARBON	R14
	RES 3.6K OHM 1/4W 5% CARBON	R26,30,32,36,39,42,53
	RES 4.7K OHM 1/4W 5% CARBON	R6,54,81

PART NUMBER	DESCRIPTION	LOCATION
	RES 5.1K OHM 1/4W 5% CARBON	R25,29,33
	RES 5.6K OHM 1/4W 5% CARBON	R56
	RES 6.8K OHM 1/4W 5% CARBON	R57
	RES 7.5K OHM 1/4W 5% CARBON	R37,40,43
	RES 8.2K OHM 1/4W 5% CARBON	R13
	RES 10K OHM 1/4W 5% CARBON	R7,48,49,78~80
	RES 12K OHM 1/4W 5% CARBON	R8,9,19
	RES 15K OHM 1/4W 5% CARBON	R38,41,44
	RES 2.7K OHM 1/4W 5% CARBON	R88
	RES 2.2K OHM 1/4W 5% CARBON	R140,141
	RES 100K OHM 1/4W 5% CARBON	R107,108
	RES 430 OHM 1/4W 5% CARBON	R89
C070159-006	RES NETWORK 4.7K OHM X 8	RP1,4~6
C070448	RES NETWORK 10K OHM X 8	RP2,3,7~9
C014384	INDUCTOR FERITE BEAD AXIAL	L2,3,6,7,11~14,47,48
C070205	INDUCTOR 0.27uH 20% AXIAL	L5,8
	INDUCTOR 1uH 10% AXIAL	L9
	INDUCTOR 1.5uH 5% AXIAL	L10
	INDUCTOR 10uH 10% AXIAL	L1
	INDUCTOR 100uH 10% AXIAL	L4
C070241-002	NOISE FILTER ZJS5101-02	L15~46
C070241-001	NOISE FILTER ED-65B102M-S	SUB FOR ABOVE
C070241-003	NOISE FILTER DST306-58B102M50	SUB FOR ABOVE
	TRANSISTOR 2N3904	Q1~8,11
	TRANSISTOR 2N3906	Q9,10
	DIODE 1N914	CR1~11
	DIODE 1N4148	SUB FOR ABOVE
C070177	DIODE 1SV69	CR12,51
C025993	CRYSTAL 2.4576 MHZ	Y1
C070246	CRYSTAL 3.579545 MHZ	Y3
C025944	CRYSTAL 32.0424 MHZ	Y2
C070517	RGB ENCODER/MODULATOR (NTSC)	MOD1
C070129	CONN 40 PIN RIGHT ANGLE	J1
C070130	CONN DB-19S HARD DISK	J6
C070131	CONN 14 PIN DIN FLOPPY DISK	J5
	CONN DB-25P RS232C	J8
	CONN DB-25S PARALELL	J7
C070134	CONN 13 PIN DIN VIDEO	J4
C070033	CONN 5 PIN DIN MIDI	J2,3
C070445	SINGLE INLINE CONNECTOR 6 PIN	J10
C070446	SINGLE INLINE CONNECTOR 8 PIN	J9
	SOCKET 40 PIN	U1,31
	SOCKET 28 PIN	U42~47
C070120	SOCKET 68 PIN LCC	U12,15
C070119	PUSH SWITCH	SW1
CA070072	PUSH SWITCH ASSY	SUB FOR ABOVE
CA070024	FLAT CABLE 34P ASSEMBLED	J11
CA070023-003	CABLE 4P ASSEMBLED	J12
C070510	JUMPER WIRE TWIST PAIR (AW626)	JP2,3
C070536-001	JUMPER WIRE TWIST PAIR (AWG22)	JP4,5

PART NUMBER	DESCRIPTION	LOCATION
C025982	IC 68000-8 CPU	U10
C025913	IC DMA, CONTROLLER CUSTOM	U1
C025915	IC GLUE, CUSTOM	U12
C025912	IC MMU, CUSTOM	U15
C025914	IC VIDEO SHIFTER, CUSTOM	U31
C025984	IC 68901, MFP	U11
	IC 1489 RS-232C, RECEIVER	U13
	IC 1488 RS-232C, DRIVER	U14
C025983	IC YM2149, SOUND	U19
C025985	IC 6850, ACIA	U20,21
	IC DYNAMIC RAM 256K X 1 <=200ns	U16~18,24,25,28~30,32~34 U38,42~61
C025988	IC PC-900 PHOTO COUPLER	U39
	IC 556, DUAL PRECISION TIMER	U37
	IC 74LS02, QUAD NOR	U40
	IC 74LS04 HEX INVERTER O.C.	U35
	IC 7406 HEX INVERTER O.C.	U8
	IC 74LS244.3 STATE LINE BUFFER	U26,27
	IC 74LS373 LATCH	U22,23
	IC 74HC74 DUAL D.F.F	U63
	IC TL497A SWITCHING REGULATOR	U62
C026028	IC WD-1772 FDD CONTROLLER	U9
	SHIELD TOP	
	SHIELD BOTTOM	
	SHIELD BOX	
	INSULATOR	
C026160-001	IC; ROM	U2
C026163-001	IC; ROM	U5
C026161-001	IC; ROM	U3
C026162-001	IC; ROM	U4
C026164-001	IC; ROM	U6
C026165-001	IC; ROM	U7
CA070097-001	PCB ASSEMBLY 1040 STF W/OUT MOD.	
CA070057-005	KEYBOARD ASSY W/ CPU -1040ST	
CA070059-002	POWER SUPPLY UL -1040 STF(M)	
C070352-002	MECH 3.5" DUAL 1M -1040STF(M)	
C070350-002	MECH 3.5" DUAL 1M -1040STF(M)	SUB FOR ABOVE
C070349-001	POWER CORD UL -1040ST	

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION ONE
INTRODUCTION

The Mega 2 and Mega 4 are Motorola MC68000 microprocessor based computers with similar architectures to the 520ST/ 1040ST line. They are styled as a main CPU unit with a detached keyboard. The Mega 2 has 2 megabytes of RAM, the Mega 4 contains 4 megabytes. Both the Mega 2 and Mega 4 have a built-in 1 Megabyte (720K formatted) 3.5 inch floppy disk drive, and an internal switching power supply with built-in cooling fan.

Since the only difference between the Mega 2 and Mega 4 is the size of its RAM, this manual will use ' Mega ' as a generic term which refers to both products.

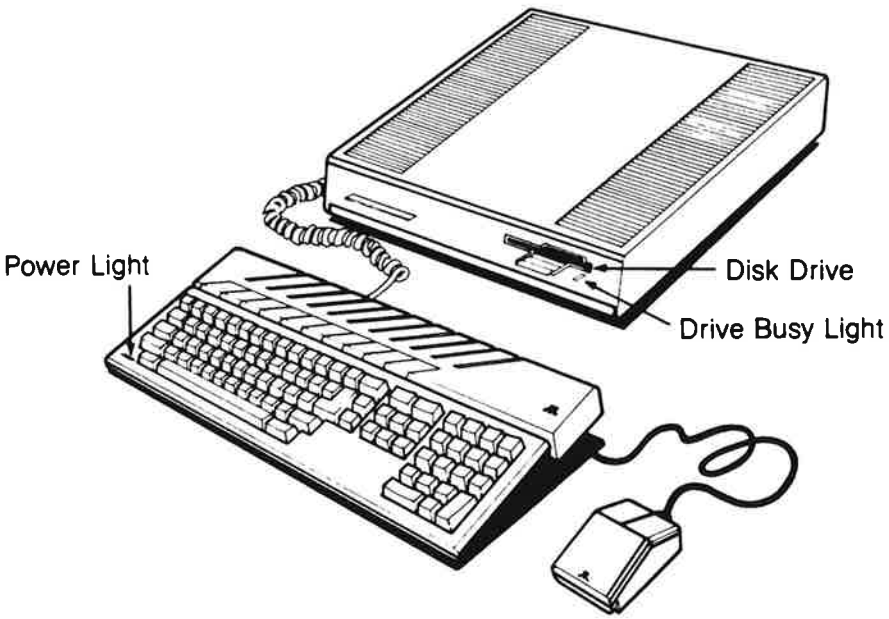


FIG. 1
MEGA COMPUTER SYSTEM

The main components of the Mega 2 and Mega 4 are:

CPU

- o Main board assembly
- o Disk drive
- o Power supply & cooling fan
- o RF Shield (upper and lower)
- o CPU Plastic case (upper and lower)

KEYBOARD

- o Keyboard assembly
- o Interface board assembly
- o Keyboard Plastics (upper and lower)

MOUSE

- o Mouse board assembly
- o Mouse Plastics (upper and lower)

CASE DESIGN

Figures 1 thru 4 shows the CPU portion of the MEGA, 5 and 6 shows the keyboard portion, and figure 7 shows the mouse.

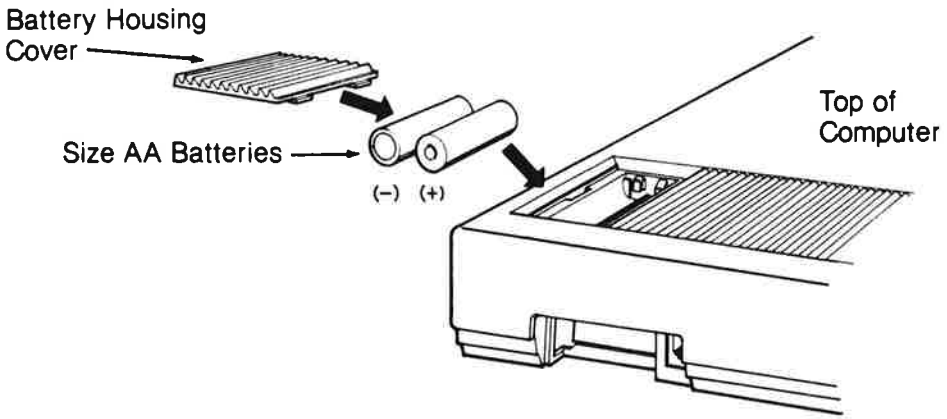


FIG. 2
BATTERY COMPARTMENT

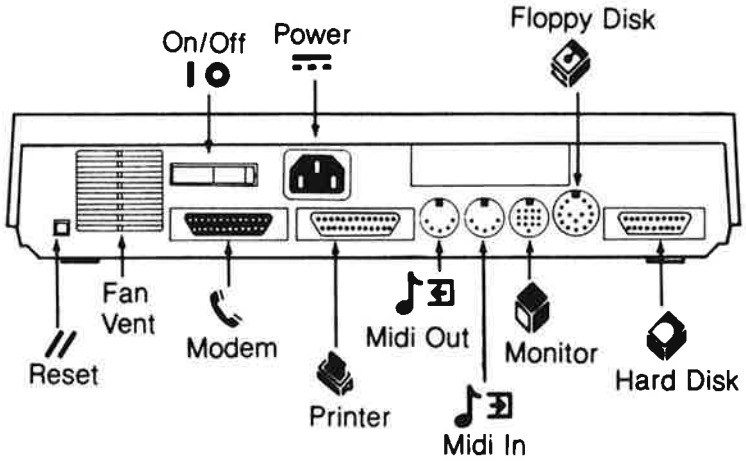


FIG. 3
BACK PANEL

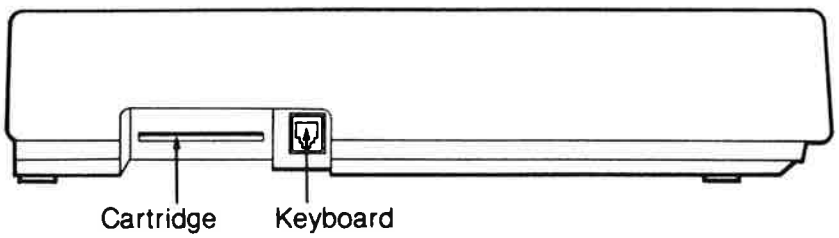


FIG. 4
LEFT SIDE PANEL

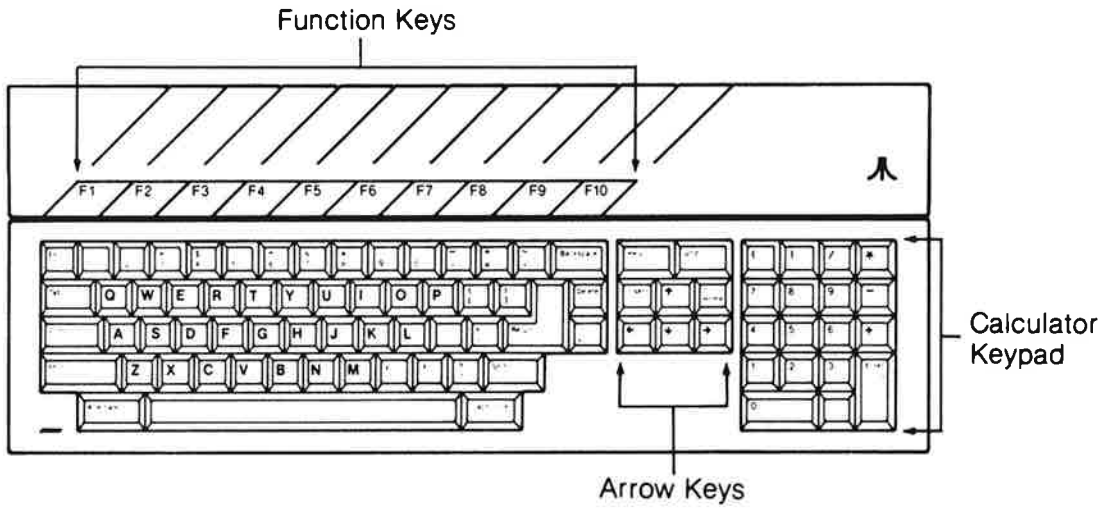


FIG. 5
TOP OF KEYBOARD

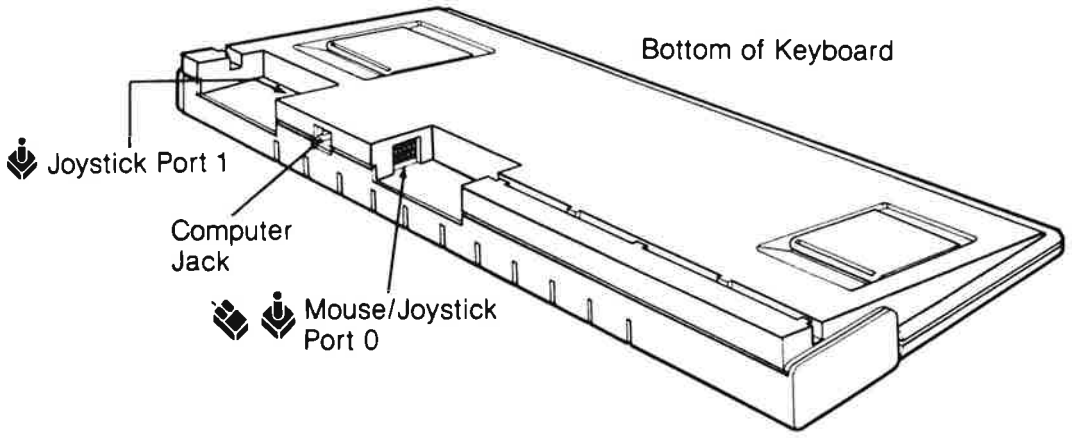


FIG. 5
BOTTOM OF KEYBOARD

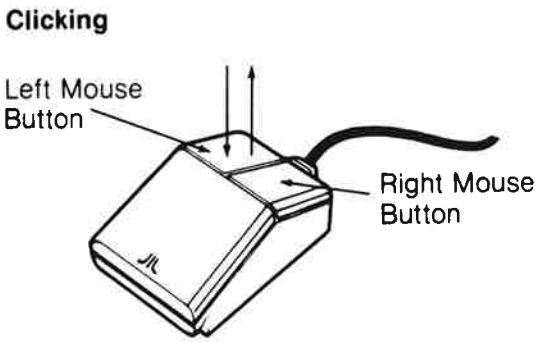


FIG. 7
MEGA MOUSE

Differences from 520ST/1040ST

- New version of TOS
- More memory requiring 74LS243 buffers on MAD lines
- Real time clock chip & support circuit
- Graphics Co-Processor (BITBLiT)
- Internal expansion connector & support circuit
- Cooling fan
- New case styling with detached keyboard

SECTION TWO
THEORY OF OPERATION

OVERVIEW

The Mega 2 and Mega 4 share a common architecture, using the same LSI chip set, and case styling. The only difference is the addition of one bank of 2 Mega-bytes of RAM, for a total of 4 Mega-bytes of RAM on the Mega 4. The hardware can be considered as consisting of a main system (central processing unit and support chips) and several Input/Output subsystems.

Main System

- MC68000 running at 8MHz
- 192 Kbyte Read Only Memory
- 2 or 4 Mega-byte Random Access Memory
- Direct Memory Access support
- System timing and Bus control
- Interrupt control

Audio/Video Subsystem

- Bit Mapped video display, using 32k bytes of RAM, relocatable anywhere in memory. There are three display modes available:
  a. 320 x 200 pixel, 16 color palette from 512 selections
  b. 640 x 200 pixel, 4 color palette from 512 selections
  c. 640 x 400 pixel, monochrome
- BITBLiT support
- Monitor interface analog: RGB, Monochrome
- Audio output: programmable sound chip with 3 voices

Input/Output Subsystems

- Intelligent Keyboard with 2 button mouse/joystick interface
- Parallel printer interface (Centronics)
- RS-232C serial interface
- DMA Port & connector for external drive
- Hard disk drive interface & Laser Printer
- Musical instrument network communication : Musical Instrument Digital Interface (MIDI).
- Real Time Clock with battery backup
- ROM Port

MAIN SYSTEM

The main system includes the microprocessing unit, main memory (ROM and RAM), system control, interrupt control, and general purpose DMA controller.

Microprocessing Unit

The Mega uses the Motorola MC68000 16 bit external/32 bit internal data bus, 24 bit address bus microprocessor, running at 8 MHz.

Glue

Glue (named because it holds the system together) is such an important component that it is involved in nearly every operation in the computer. The functions may be summarized as follows:

Clock dividers-- takes the 8 MHz clock and outputs 2 MHz and 500 KHz clocks.

Video timing-- Blank, DE (Display Enable), Vsync, and Hsync are used to generate signals for the video display. There is a Read/Write register in Glue which may be written to configure for 50 or 60 Hz operation (done by the Operating System).

Interrupt priority-- interrupts from the MFP and video timing are coded into four levels of priority on outputs IP11 and IPL2 to the 68000. These levels correspond to no interrupts, MFP interrupts, VSYNC interrupt, HSYNC interrupt.

Signal and Bus arbitration-- Glue decodes addresses to generate chip selects to the 6850s, MFP, DMA Controller, Programmable Sound Generator, Memory Controller, and ROMs. It receives signals from the MFP, DMA, Memory Controller, to synchronize data transfer. It arbitrates the bus during DMA transfers to prevent CPU and DMA devices from interfering with each other (see DMA below).

Illegal condition detection--Glue asserts Bus Error (BERR) if certain conditions are violated, such as writing to ROM, writing byte sized data to a word sized register, or writing to system memory when the processor is in user mode. Also occurs if a device does not respond within the required time limit. For example, the CPU tries to read from memory and the Memory Controller does not assert DTACK.

Main Memory

Main memory consists of 192 kbytes of ROM and one or two banks (2 Mega-byte each) of dynamic RAM. In addition, the cartridge slot allows access to 128 Kbytes of ROM. All memory is directly addressable. The components of the memory system are: ROM, RAM, RAM buffers, Memory Controller, and Glue. The Operating System resides mostly in ROM, with optional segments loaded from disk into RAM.

RAM is organized as 16 bit words and may be accessed 16 bits at a time or 8 bits at a time. Even numbered addresses refer to the high 8 bits of a word and odd addresses refer to the low 8 bits. RAM is made up of 1 Megabit X 1 chips; in the Mega 2 there are 16 chips, giving 2 Mbytes, while in the Mega 4 there is an additional bank of 16 chips, giving two times the memory, or 4 Mbytes.

RAM memory map:

000008-000800	System memory (priveliged access)
000800-1FFFFF	low bank
200000-3FFFFF	high bank (Mega 4 only)

Note: the first 8 bytes of ROM are mapped into addresses 0-7. These are reset vectors which the 68000 uses on start-up.

The Operating System is located in two 1Meg x 8 ROM chips in current versions (192k).

Memory Controller--takes addresses from the address bus and converts to Row Address Strobe (RAS) and Column Address Strobe (CAS). All RAM accesses are controlled by this Atari proprietary chip, which is programmable for up to 4 Megabytes of memory. The Operating System determines how much memory is present and programs the Memory Controller at power-up. The Memory Controller refreshes the dynamic RAMs, loads the Video Shifter with display data, and gives or receives data during direct memory access (DMA).

Glue--decodes addresses for RAM and ROM and asserts output signals to enable these devices (also decodes addresses for most hardware registers to provide chip selects, as well as many other functions. See Glue description above.).

Direct Memory Access

Direct memory access is provided to support both low speed (250 to 500 Kilobits/sec) and high speed (up to 8 Megabits/sec) 8bit device controllers. The floppy disks transfer data via low speed DMA and the hard disk (or other devices on the hard disk port) transfer at high speed. For DMA to take place, the Memory Controller is given the address of where to take data from or put data in RAM, the DMA Controller is set up (which channel, high speed or low speed, and how many bytes) and the peripheral is given a command to send or receive data. The entire block of data (the size must be given to the DMA Controller and the peripheral before the operation starts) is then transferred to or from memory without intervention by the CPU.

For example, in a transfer of a sector from the floppy to memory, the floppy controller will signal the DMA Controller that a byte is ready by asserting FDRQ, the DMA chip will read the byte and signal Glue, Glue will signal the Memory Controller, and the Memory Controller will read the byte from the DMA Controller and place it in the address which was set up previously. The DMA Controller will then wait for the next byte from the floppy controller, and the process will repeat until the specified number of bytes has been transferred. Transfers from memory to floppy are similar. The floppy initiates every transfer by requesting data on FDRQ.

At high speed (hard disk port), there is a difference: as a byte is ready to transfer to or from the DMA chip, the DMA Controller will assert ACK to let the peripheral know the byte is available or has been read. The DMA Controller can store up to 32 bytes in internal memory. This is necessary if the 68000 is using the bus, and the DMA must wait to transfer to memory. Data may be input from the port without being lost or slowing down the transfer speed.

MFP Interrupt Control

The 68901 MFP handles up to 16 interrupts. Currently all but one are used. Each interrupt can be masked off or disabled by programming the MFP. The 8 inputs are also directly readable by the CPU. When the MFP receives an interrupt input, or generates an interrupt internally, if the interrupt is enabled, MFPINT will be driven low. When the CPU is ready to respond, it signals interrupt acknowledge (FC0-2 high and VMA low) and Glue will assert IACK (interrupt acknowledge). The MFP will assert DTACK and put a vector number on the data bus, which the CPU will read and use to calculate the address of the interrupt routine.

The interrupts controlled by the MFP are: monochrome monitor detect (MONOMON), RS232 (including CTS, DCD, RI), disk (FDINT and HDINT), parallel port BUSY, display enable (DE, equals start of display line), 6850 IRQs for keyboard and MIDI data, and MFP timers.

Not all I/O operations use interrupts. The CPU can also poll the MFP while waiting for an operation to complete. The MFP has four timers, used by the Operating System for event timing and used by the RS232 port for transmit and receive clocks.

AUDIO/VIDEO SUBSYSTEM

The video subsystem consists of the video display memory, the Memory Controller, Glue, a graphics control chip (Video Shifter), a graphics processing unit (BITBLiT), and a discrete section to drive the video output. The audio subsystem consists of a Programmable Sound Generator chip with a transistor output amplifier.

Video Shifter

There are 16 color palette registers in the shifter. All 16 are may be used in low resolution, 4 may be used in high resolution, and only one is used in high resolution (actually, only bit 0 of register 0 is used for inverse/normal video). Each palette is programmed for 8 levels of intensity of red, blue, and green, so there are 8 x 8 x 8 = 512 colors possible. For a given pixel, the color which is displayed is taken from the palette referred to by getting information from each logical plane (see description of video display memory below). The shifter will output the red, green, and blue levels specified by that palette; note there are three outputs for each color. Each output is either on or off. Thus, the number of possible output levels is 2 to the 3rd power = 8. The three outputs are summed through a resistor network to proportion the voltage level to give 8 equal steps. In monochrome mode, the color palettes are bypassed and there is a separate output.

Video Display Memory

Display memory is part of main memory with the physical screen origin located at the top left corner of the screen. Display memory is configured as 1, 2, or 4 (high, medium, or low resolution) logical planes interwoven by 16 bit words into contiguous memory to form one 32 Kilobyte physical plane starting at a 256 byte half page boundary. The starting address of display memory is placed in the Memory Controller's Video Base Address register by the Operating System or application. The Memory Controller will load display information into the Video Shifter 16 bits at a time, and the Video Shifter will decode this information to generate a serial display stream. In monochrome mode, each bit represents 1 pixel on or off. In color, bits are combined from each plane to generate the correct level of red, green, and blue.

For example, in low resolution (4 planes) 4 words are loaded into the Video Shifter for each word (16 pixels displayed on the screen. The Video Shifter combines bit 0 from each word to form a four bit number (0-15), and takes the color from the palette referenced by that number (e.g. 0101=5, use color from palette register 5) and outputs those levels, then takes bit 1 from each plane and outputs the color from the palette referenced by those four bits, etc.

Glue

Glue provides timing control to the Memory Controller, video output, and monitor/RF output. VSYNC input to the Memory Controller causes the starting address of the display memory to be reloaded into the address counter during vertical blanking. DISPLAY ENABLE (DE) tells the Memory Controller and Video Shifter that a display line is being scanned and data should be loaded into the Video Shifter. BLANK shuts off the video output from the Video Shifter during periods when the scan is not in a displayable part of the screen. VSYNC and HSYNC both go to the monitor output and RF modulator. These signals synchronize the monitor or T.V. vertical and horizontal sweep to the display signal.

Memory Controller

In addition to the inputs from Glue mentioned above, there are two output control signals associated with video. DCYC strobes data from display memory into the Video Shifter. CMPCS (color map select) is active only when changing the color attributes in the color palettes.

Sound Synthesizer

The YM2149 Programmable Sound Generator (PSG) produces music synthesis, sound effects, and audio feedback (e.g. alarms and key clicks). The clock input is 2 MHz; the frequency response range is 30 Hz to 125 KHz. There are three sound channels output from the chip, which are mixed and sent to the monitor speaker.

The PSG is also used in the system for various I/O functions relating to printer port, disk drive, and RS232.

Atari Blitter

This is a DMA device that moves block of memory data from a source location to a destination location through a given logic operation. Single or multiple word increments and decrements are provided for transfer to destination. There are 16 possible logic operation rules associated with the merging of source and destination data. In addition, with the 16 word patterns ram and three 16 bit end-mask registers, the blit can also be used to perform operations such as area seed filling, pattern filling, brush line drawing, text and graphic transformations, etc.

For more information, please refer to the user manual which is included in the Developer Kit.

Real Time Clock with Battery Backup

This device has counters for Time and Calendar built-in. Clock data are expressed with BCD code. The lower four address and data lines are used to program the device and access the clock through signal lines RTCCS, RTCRD, RTCWR which generated from a decoder. A RESET line is also provided to reset the chip when the system is reset. The main clock supplied to the device is a 32.768 Khz oscillator which will be adjusted by a trimmer condenser so that it will output through the CLKOUT line a standard clock signal of 16.384 Khz. In addition, a 3V battery backup can be used to keep the clock running during power down.

For more detail, please refer to the application manual from the manufacturer (RICOH part number RP5C15)

Video Interface

The two types of interface are provided in the Megas are analog RGB and monochrome. The presence of a monochrome monitor is detected by the MONOMON input (when a monochrome monitor is connected, it will be low). The possible displays are:

Monochrome: single emitter follower amplifier driving the output of the Video Shifter.

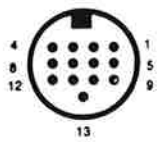
RGB: resistor network sums outputs for each color. The three colors each have an emitter follower amplifier to drive output.

Monitor Inputs:

Hsync--TTL level, negative, 3.3 k ohm.
Vsync--TTL level, negative, 3.3 k ohm.
Monochrome--digital 1.0V P-P, 75 ohm.
R,G,B--analog 0-1.0V P-P, 75 ohm.
Audio--1V. P-P, 1k ohm.

Monitor

1 — Audio Out
2 — Composite Sync
3 — General Purpose Output
4 — Monochrome Detect
5 — Audio In
6 — Green
7 — Red
8 — Plus 12-Volt Pullup
9 — Horizontal Sync



10 — Blue
11 — Monochrome
12 — Vertical Sync
13 — Ground

FIG. 8
MONITOR PORT

Musical Instrument Communication

The Musical Instrument Digital Interface (MIDI) allows the integration of the Mega with music sysnthesizers, sequencers, drum boxes and other devices possessing MIDI interfaces. High speed (31.25 Kilobaud) asynchronous current loop serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port). MIDI specifies that data consist of 8 data bits preceded by one start bit and followed by one stop bit.

Communication takes place via a 6850 ACIA. The CPU reads and writes to the 6850 in response to interrupts which are passed from the 6850 to the MFP interrupt controller. The system is interfaced to the outside via two inverters on the transmit side and an LED/photo-transistor chip on the input side. The input signal is routed around through two inverters to the output connector where it is called MIDI THRU in order to allow chaining of multiple devices on the MIDI bus.

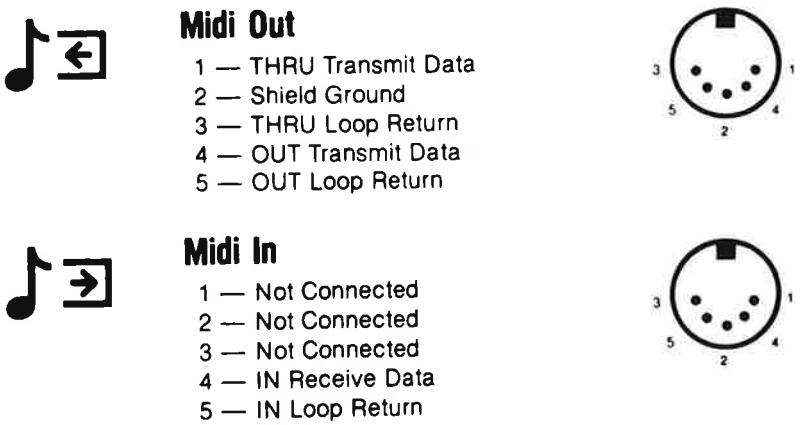


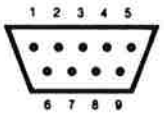
FIG. 9
MIDI PORTS

Intelligent Keyboard

The keyboard transmits make/break key scan codes, ASCII codes, mouse data, joystick data, in response to external events, and time-of-day data (year, month, day, hour, minute, second) in response to requests by the CPU. Communication is controlled on the main board by a 6850 device and on the keyboard assembly by the 1MHz 8 bit HD6301 Microcomputer Unit. The HD6301 has internal RAM and ROM. Included in ROM are self-test diagnostics which are performed at power-up and whenever the RESET command is sent over the serial communication line by the CPU. The MC6850 is read and written to by the CPU in response to interrupts which are passed to the CPU by the MFP interrupt controller.

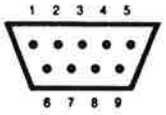
The 2 Button Mouse is an opto-mechanical device with the following characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second and a maximum pulse phase error of 50 percent. The joystick/mouse port has inputs for up, down, left, right, right button, left button. The right button equals the joystick trigger, and the left button is wired to the second joystick port trigger. The joystick has four directions (up, down, etc.) and one trigger.

Mouse / Joystick



1 — Up/XB
2 — Down/XA
3 — Left/YA
4 — Right/YB
5 — Not Connected
6 — Fire/Left Button
7 — + 5VDC
8 — Ground
9 — Joy1 Fire/Right Button

Joystick



1 — Up
2 — Down
3 — Left
4 — Right
5 — Reserved
6 — Fire Button
7 — + 5VDC
8 — Ground
9 — Not Connected

FIG. 10
MOUSE/JOY PORT

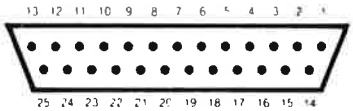
Parallel Interface

The parallel port is primarily intended as a Centronics type printer interface, but can also be used as a general purpose I/O port. Centronics STROBE and BUSY are supported. BUSY is read by the MFP chip. Data and strobe signals are output by the YM2149 PSG chip. Not all Centronics printers are compatible with this port. The current loading on the data lines should not exceed 2.3 mA. (This corresponds to a 2.2k ohm resistor pull-up on the printer side.)

The port can be programmed to be input or output. The PSG chip is read directly by the CPU, with Glue doing address decode to provide chip select.

Printer

1 — STROBE Output
2 — Data 0
3 — Data 1
4 — Data 2
5 — Data 3
6 — Data 4
7 — Data 5
8 — Data 6
9 — Data 7



10 — Not Connected
11 — BUSY Input
12-17 — Not Connected
18-25 — Ground

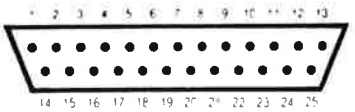
FIG. 11
PRINTER PORT

RS232C Interface

The RS232C interface provides asynchronous serial communication with five handshake control signals: Request to Send and Data Terminal Ready are output by the PSG chip; Clear to Send, Data Carrier Detect, and Ring Detect are input to the MFP chip. The MFP contains a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) which handles data transmission and reception. The 2.4576 MHz clock to the MFP is divided by the timer D (pin 16) output of the MFP to provide the basic clock for receiver and transmitter. Data rate of 50 to 19200 bits per second are supported. 1488 line drivers and 1489 line receivers with +/- 12v. supply meet the EIA RS232C standard for electrical interface.

Modem

1 — Protective Ground
2 — Transmitted Data
3 — Received Data
4 — Request to Send
5 — Clear to Send
6 — Not Connected
7 — Signal Ground
8 — Data Carrier Repeat
9-19 — Not Connected



20 — Data Terminal Ready
21 — Not Connected
22 — Ring Indicator
23-25 — Not Connected

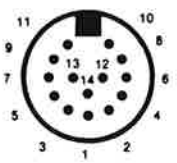
FIG. 12
RS232 PORT

Disk Drive Interface

The Mega computers have a built-in floppy disk controller (a Western Digital 1772) and logic for selecting up to two single or double sided drives. The Mega has one built-in floppy disk drive and provision for one external disk drive. The Western Digital WD1772 Controller services both drives. Drive and side selection is done by outputs on the YM2149 PSG chip. The CPU reads and writes to the 1772 through the DMA Controller. The 1772 interrupts the CPU on the INTR line, via the MFP interrupt controller. The 1772 accepts high level commands, such as seek, format track, write sector, read sector, etc. and passes data to the DMA Controller (see DMA controller under Main System, above, for details on DMA transfer). The 1772 interrupts the CPU when the operation is complete. The CPU is freed from much of the overhead of disk I/O.

Floppy Disk

1 — Read Data
2 — Side 0 Select
3 — Logic Ground
4 — Index Pulse
5 — Drive 0 Select
6 — Drive 1 Select
7 — Logic Ground
8 — Motor On
9 — Direction In
10 — Step



11 — Write Data
12 — Write Gate
13 — Track 00
14 — Write Protect

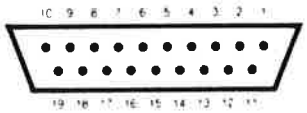
FIG. 13
EXTERNAL FLOPPY PORT

DMA Port; Hard Disk Interface

The hard disk drive interface is provided through the DMA controller; the hard disk controller is off-board and is board and is sent commands via an SCSI-like (Small Computer System Interface) command parameter block. Data is transferred via DMA. Writing to the external controller causes HDCS (Hard Disk Chip Select) to go low and CA1 to go high. DMA transfers are controlled by the external device. When data is available, or the device is ready to accept data, HDRQ will be driven high by the external controller. The DMA chip must respond within 250 nanoseconds with ACK (low) to acknowledge that data is on the bus or has been read from the bus. The Memory Controller feeds data to or accepts data from the DMA Controller. Transfers can take place at up to 1 Mbyte/second.

Hard Disk

1 — Data 0
2 — Data 1
3 — Data 2
4 — Data 3
5 — Data 4
6 — Data 5
7 — Data 6
8 — Data 7
9 — Chip Select
10 — Interrupt Request
11 — Ground
12 — Reset



13 — Ground
14 — Acknowledge
15 — Ground
16 — A1
17 — Ground
18 — Read/Write
19 — Data Request

FIG. 14
EXTERNAL HARD DISK PORT

SYSTEM STARTUP

After a RESET (power-up or reset button) the 68000 will start executing at the address pointed to by locations 4-7, which is ROM (Glue maps 8 bytes of ROM at FC0000-7 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM (FC0000-FEFFFF). The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse).
2. Read the longword at cartridge address FA0000. If the data read is a "magic number", execute from the cartridge (diagnostic cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations were previously written), initialize the memory controller, and continue running the application which was running before the reset if it was a warm start.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.
6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if succeeded.

SYSTEM ERRORS

The 68000 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen (mushroom clouds in older versions of disk loaded operating system). The number of bombs equals the number of the exception which occurred.

System errors may or may not be recoverable. Errors in loading files from disk will cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

NUMBER OF BOMBS AND MEANINGS
(No. 26,28,30, and 64-79 will not bomb, as they are legitimate.)

2 Bus Error. Glue asserted bus error or CPU detected an error.
3 Address Error. Processor attempted to access word or long word sized data on an odd address.
4 Illegal Instruction. Processor fetched an instruction from ROM or RAM which was not a legal instruction.
5 Zero Divide. Processor was asked to perform a division by zero.
6 Chk Instruction. This is a legal instruction, if software uses this, it must install a handler.
7 Trapv Instruction. See Chk instruction.
8 Privilege Violation. CPU was in user mode, tried to access a location in supervisor address space.
9 Trace. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.
10 Line 1010 Emulator. CPU read pattern 1010 as an instruction. Provided to allow user to emulate his own instructions.
11 Line 1111 Emulator. See Line 1010 Emulator.
12-23 Unassigned, should be no occurrence.
24 Spurious Interrupt. Bus error during interrupt processing.
25-31 Autovector Interrupt. Even numbered vectors are used, others should have no occurrence.
32-63 TRAP Instruction. The CPU read instruction which forced exception processing.
64-79 MFP interrupts.
80-255 User interrupts.

Note: If you have an error message such as "TOS ERROR 35", then the possible errors are:

1- The file in progress is bad.
2- The total number of folders in the system has exceeded the 40-folder limit. However, there is a program which can be used to extend this limitation on folders.
3- No handles left or too many open files.

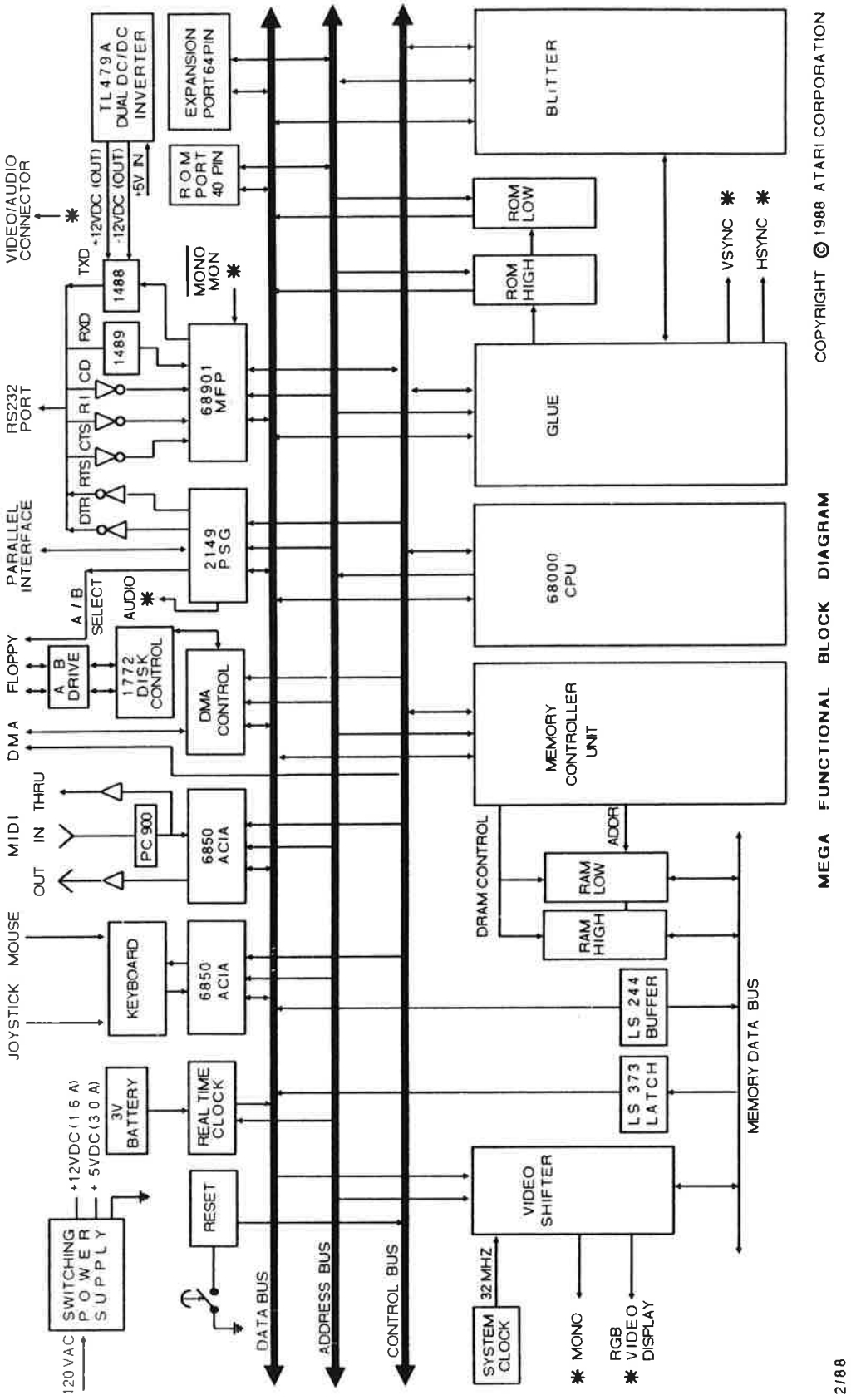


FIG. 15
FUNCTIONAL BLOCK DIAGRAM

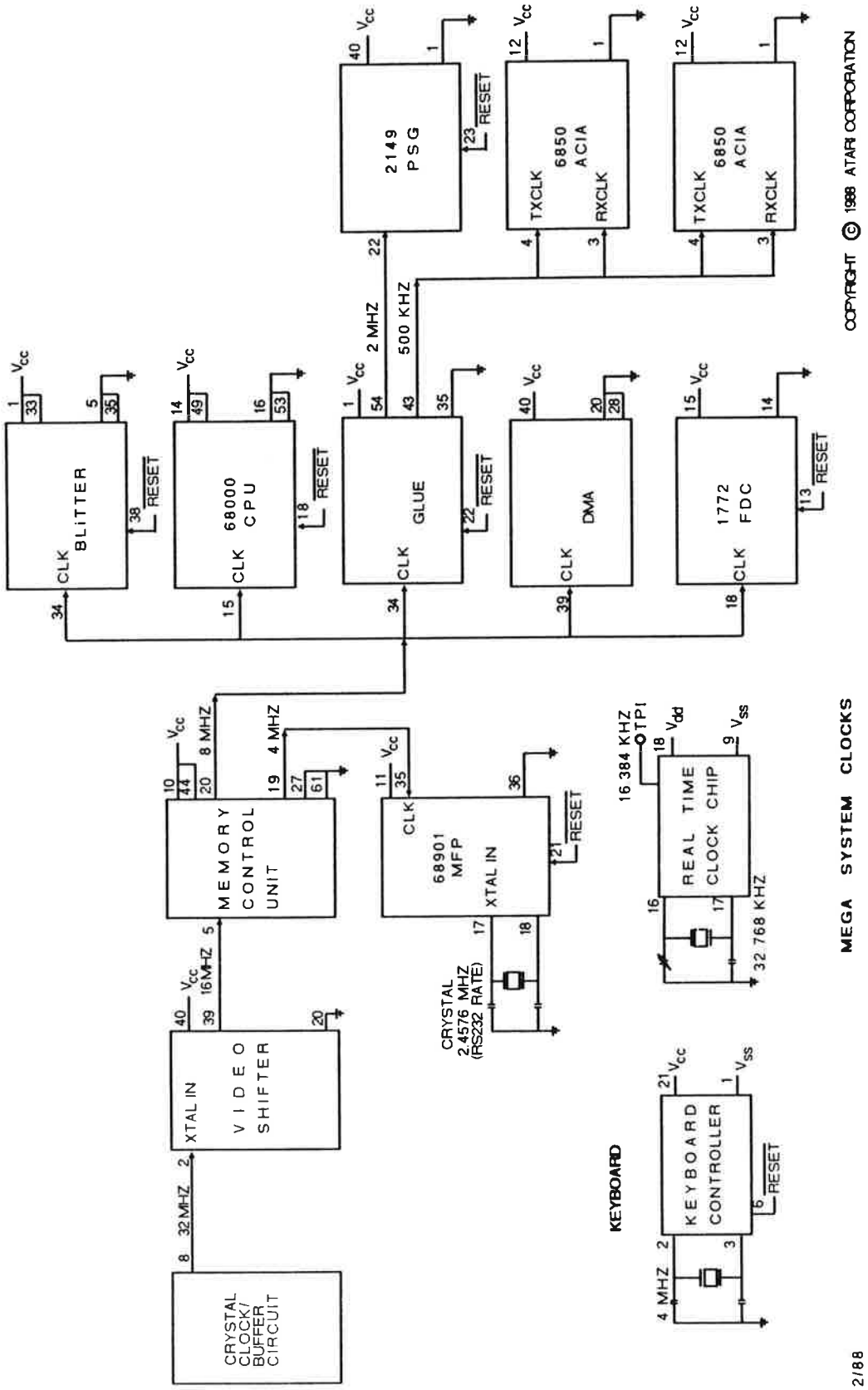


FIG. 16
SYSTEM CLOCKS

SECTION THREE
TESTING

OVERVIEW

This section pertains to the test equipment, diagnostic software, and test procedures used to verify correct operation and repair the Mega/ST computers. The diagnostic cartridge should be used if possible. If the unit gives no display or RS232 output when running the cartridge, see "Troubleshooting a Dead Unit" below.

Since the level of complexity in the Mega/ST system is high, it shouldn't be expected that this document can cover all possible problems or pinpoint the causes; rather, the intent here is to give a systematic approach which a technician can use to narrow down a problem to its most likely source. Experience in troubleshooting computer systems is assumed. Knowledge of the 68000 processor may be helpful. Economics will be an important consideration; due to the low cost of the Mega/ST computer line, little time can be justified in troubleshooting down to the component level when it may be cheaper to exchange the entire sub-assembly. Many of the more expensive (and critical) components maybe socketed, making verification and replacement faster.

TEST EQUIPMENT

The following equipment will be needed to test the Mega/ST computer:

* Atari SC1224 RGB Monitor (or similar)
* Atari SM124 Monochrome Monitor (or similar)
* Atari SF354 or SF314 Floppy Disk Drive
* Mega/ST Port Test Fixture
* Mega Expansion Test Fixture (Mega only)
* RS232 Loop-Back Connector
* MIDI Loop-Back Cable
* Mega/ST Test Diagnostic Cartridge (Revision 4.0)
* Diskettes (2)
* RS232 terminal (or Mega in VT52 emulator mode)

In addition, the following items will be necessary to troubleshoot and repair failed computers:

* Oscilloscope (100MHz Reccommended)
* Digital Multimeter, 1% FS (or better)
* Small Hand Tool, & Soldering Iron
* Spare Parts

TEST CONFIGURATION

With the power switch off, install the Diagnostic Cartridge (IMPORTANT--if the cartridge does not have the plastic enclosure, BE SURE THE CARTRIDGE IS INSTALLED WITH THE CHIPS FACING DOWN). Connect cables from test fixture into the hard disk port, parallel port, and joystick / mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the RS232 and MIDI loopback connectors into their ports. Plug the color monitor into the monitor output (a monochrome can be used instead).

Power on the unit. Some tests will be run automatically; in a few seconds the menu screen should appear. If the screen appears, skip down to " Mega/ST Diagnostic Cartridge ", below. If not, read next section "Troubleshooting a Dead Unit".

If the unit is being used as a terminal for a host computer, it should be disconnected from the host before using the diagnostic; otherwise, the host may think someone is logging on, and will send messages which will act like keystrokes input to the diagnostic.

TROUBLESHOOTING A DEAD UNIT

In the event that the system is correctly configured and powered and no display appears, this is the procedure to use for determining the problem. This assumes elementary steps have been taken, such as checking the LED in the forward left corner of the computer to verify the unit is powered and making sure the monitor is working.

1. Connect a dumb terminal to the RS232 port of the unit under test (U.U.T.). You can use an Mega/ST running the VT52 terminal emulator program--see the owner's manual for setting up VT52. The cable should connect pin 2 (serial out) of the U.U.T to pin 3 (serial in) of the terminal, and vice versa. Connect pin 7 (ground) to pin 7. The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity (this is the default condition for the VT52 emulator).

Insert the Diagnostic Cartridge into the U.U.T., and power on the unit. If the Diagnostic Cartridge messages appear on the display of the terminal, use the diagnostic to troubleshoot the computer. If not, the computer will have to be disassembled to troubleshoot. Refer to "Diagnostic Cartridge" below for information on using the cartridge.

If no activity is seen on the RS232 port or display, continue with (2) next page.

2. Disassemble the computer so that the printed circuit board is exposed (see Section 4, Disassembly). Power up the computer. Using an oscilloscope, verify the 8MHz clock to the 68000 CPU (pin 15). Replace oscillator if necessary. Then check pin 17 (HALT) of the 68000 CPU. It should be a TTL high. If so, go on to 3 below. If not, the CPU is halted. The reasons may be: (1) bad reset circuit, (2) double bus error, 3) bad CPU. Check (1) by observing signal on input of the two inverters on the HALT line. Check (2) by observing pin 22 of the CPU (BERR) as the unit is powered on. It should be high always. If there are logic low pulses, some component is malfunctioning and Glue is generating the error. Verify the clocks to Glue and Memory Controller and replace these components to verify them (if socketed). If still failing, the CPU is unable to read ROM or there is a component which is not responding to a read or write by the CPU, probably the MFP 68901 or DMA Controller. The MFP should respond to an MFPCS with DTACK. The DMA chip should respond to FCS by asserting RDY. There is no way to check (3) other than by elimination of the other two possibilities, although a hot CPU (too hot to touch for more than a second) strongly indicates a bad CPU.

3. If the CPU is not halted, it should be reading instructions from ROM (cartridge, if installed) and data and address lines will be toggling. (If not, replace CPU.) At this point, there is the possibility that both the video and RS232 subsystems are failing. Verify the output of the MFP chip (pin 8) while powering on the unit with the cartridge installed. If data is being sent, trace it through the 1488 driver. Note that + and - 12v. is required for RS232. If all looks good, there may be something wrong with the connection to the terminal.

Verify also the output of the Video Shifter. If using an RGB monitor, check the outputs to the summing resistors (if external) for R, G, and B. Note that if BLANK is not going high, no picture will be possible. If using monochrome, check output pin 30. Also check the input to the MFP, pin 29, MONOMON. Note that if the CPU does not read a low on this signal on power-up, it will cause RGB output on the Video Shifter.

If the Video Shifter is outputting a signal, but the picture is unreadable, there is probably a problem with screen RAM. The cartridge should be used to diagnose this problem, with the RS232 terminal as a display device.

MEGA/ST DIAGNOSTIC CARTRIDGE

The diagnostic cartridge is used to detect and isolate component failures in the computers (520/1040 and Mega). There are several revisions; this document refers to revision 4.0. Users of earlier versions should refer to the appropriate Troubleshooting Guide. This section gives a brief guide to use with a description of each test, error codes or pass/fail criteria, and recommendations on repair.

Power-up

The diagnostic program performs several tests on power-up. In particular, the message "Testing MFP, Glue timing, Video will appear, and the screen will appear scrambled for a few seconds before the menu is printed. The screen will turn red (dark background in monochrome) if an error occurs in the initial testing, with a message indicating the failure. The lowest 2 Kbytes of RAM is tested on power-up; if a location fails, the error will be printed to the RS232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there is no stack or system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen may turn red). Repair RAM.

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS232 port. The diagnostic program looks for keystrokes from the RS232 device.

If the display is unreadable, the RS232 terminal should be used. All messages are printed to the RS232 port as well as the screen.

Test Menu

The normal screen will be dark blue with white letters. The test title and revision number are displayed at the top, with the amount of RAM and keyboard controller revision below, and a test menu below that. To select tests, the user types the keys corresponding to those tests, and then the return key. Many iterations of the test or tests chosen can be run by typing in the number of cycles just before typing RETURN. Typing a zero will cause the test sequence to run continuously. To stop a cycle before completion, hit the escape key (there may be some delay in some tests before the test stops). As each cycle completes, the total numbers of cycles will be displayed on the screen.

MAIN MENU

Mega and ST Field Service Diagnostic Test Rev. 4.0
© 1987, Atari Corporation
4M RAM Keyboard revision 2 60 Hz OS Version 2 USA NTSC

R	RAM Test	O	O.S. ROMs	C	Color
K	Keyboard	M	MIDI	S	Serial Port
A	Audio	T	Timing	D	DMA Port
F	Floppy Disk	P	Printer/Joy Ports	H	High resolution

G Graphics chip (Blitter)
L Real-time clock
X Expansion connector

Q Run All Tests
Z Run Internal tests (R,O,C,K,A,T,L,G)

E Examine/Modify memory
B Set RS232 rate
V Toggle video output--50/60 Hz
? Help

Enter letter(s), and RETURN

The "G", "L", and "X" selections will be highlighted if these devices are found at start-up time. These should be present in Mega systems only. (The "X" selection requires the expansion test fixture be installed, which requires disassembly). If these selections are made when not highlighted, the test will check for their presence, and test if found.

The 'Q' selection sequences through all the tests except for High resolution monitor. The 'Z' selection sequences through RAM, ROM, Color, Keyboard, and Timing tests. Selection 'E' enables the operator to examine or modify RAM or hardware registers. The 'B' enables the operator to change the baud rate on the RS232 port. Pressing the up arrow increases it, pressing the down arrow decreases it.

Pressing '?' or the HELP key brings up a brief synopsis of the cartridge functions.

After a test or series of tests completes, the pass/fail status and error report, if any, will be displayed. Press the space bar to return to the menu.

If multiple tests are selected, the sequence can be halted before completion by pressing the ESC key. At the completion of the current test, the sequence will halt, with the options of either continuing or returning to the menu. In some cases there will be a considerable delay before the current test completes and the keystroke is detected. (Up to 3 minutes with 4 meg of RAM.)

Summary of Tests

RAM TEST

RAM is tested in three stages: low 2 kbytes, middle (up to 64k), and from 64k to top. The test patterns used are: all 1s, all 0s, a counting pattern (data=low word of the address), reverse counting pattern (data=complement of address low word). The counting pattern is copied from the top and bottom of a 32 Kbyte buffer into the current 32 Kbytes of video RAM, then shifts video RAM to a new area, verifies the pattern, and repeats the test, until the top of RAM is reached. Finally, addressing at 64k boundaries is checked by writing unique pattern in last 256 bytes of each 64k block.

If an error occurs, the error code is displayed, followed by the address, data written, data read, and the bits which did not agree. E.g.: " R2 45603E W:603E R:613C bad bits: 1,8".

In units having more than one bank (i.e., 1040ST, MEGA4) the address as well as the bit position must be used to find the correct chip. The following table gives a correspondence between the addresses and banks for various models:

	520	1040	Mega 2	Mega 4
0-7ffff	bank 0	bank 0	bank 0	bank 0
80000-fffff		bank 1	bank 0	bank 0
100000-1fffff			bank 0	bank 0
200000-3fffff				bank 1

(A bank is a 16 bit wide group of RAMs. A bank may consist of 256k bit chips--256k x 16 = 4 Mbit or 512k bytes--or 1Mbit chips--1Mbit x 16 = 16 Mbit or 2 Mbytes.)

RAM ERROR CODES

Except where noted, repair by replacing the RAM chip corresponding to the indicated bit(s).

R0--low memory failed while setting up to run test.

R1--failed walking 1s or 0s.

R2--failed address (counting pattern).

R3--failed 64k boundary test. Probable failure in Memory Controller.

R4--failed while displaying area tested (video RAM).

ROM TEST

This test reads the configuration bytes of the operating system to determine the version, language/country, and TV standard (PAL or NTSC). All bytes from operating system ROMs are then read and the checksums are calculated. These values are compared against known value with checksums for this version to determine if good or bad. Six checksums are displayed, although there may be only two ROMs in the machine (some machines have six 128K ROMs; some have two 1 meg ROM'S).

The test fails if the checksum calculated does not match the checksum expected for the configuration byte found (e.g. Version 2, French). Incorrect checksums are indicated by a message. If an error is displayed, replace the corresponding ROM. In a two ROM set, replace the low ROM if any of L0, L1, or L2 showed an error, or replace the high ROM if any of H0, H1, or H2 showed an error.

New revisions of TOS will cause this test to fail if not incorporated into the current version of the diagnostic. If you receive TOS revisions before receiving the diagnostic revision, it will be necessary to verify the checksums yourself.

COLOR TEST

This test verifies the Video Shifter. Seven color bands are displayed: red, green, blue, cyan, magenta, yellow, and white. Each band consists of 8 levels of intensity. All 16 color palettes are represented, each palette is a vertical strip across the screen (strips should not be discernable, but each color should be a straight line across the screen). Because of the tight timing involved, keystroke interrupts will cause the display to jitter.

The operator should see that there are no gaps or missing scan lines in the display. If lines are missing, check the three outputs on the Video Shifter for that color, and verify the values of the resistors on the output. Too low a brightness setting on the monitor will cause the monitor not to distinguish between fine levels, making it appear there are only four levels being output.

The Video Shifter has three outputs for red (R0, R1, R2), green (G0, G1, G2) and blue (B0, B1, B2). Each of these triples is summed together by a resistor network to give eight levels of intensity for each color, depending on which of the outputs are on. The values of the resistors give different weight to each output. The value of the resistor at R0 is twice that of R1, which is twice that of R2. This allows us to get 8 equal steps on the summed outputs. For example, R0 on , R1 and R2 off = 1/8, R0 off, R1 and R2 on = 7/8. This signal then passes through a transistor amplifier, and from there to the video monitor connector. NOTE : this resistor network is incorporated into the full custom chip in later versions of the video shifter (C101608). Video shifter which has part number C101608 or C070713 has pin 1 connected to to signal line BLANK. Shifter with part number C025914 will have pin 1 connected to a pull-down resistor R144,10K, and signal line BLANK will be connected to diodes D9, D10, D11.

Symtoms and fixes:

1. Missing primary color. Check the output of the transistor amplifier. Q6 is blue, Q7 is green, Q8 is red. Look for a staircase pattern (eight levels of intensity). If the signal is there, trace forward to the video connector, if not, trace backward to the Video Shifter, until the faulty component is found.

2. Primary colors present, secondaries missing or incorrect. Replace the Video Shifter.

3. Coarse change in intensity (not a smooth dark to light transition). Replace Video Shifter or look for a short on the output of one of the three color outputs for the appropriate color.

4. Specks or lines on the screen. This can be caused by bad RAM; if RAM has been tested and is good, replace the Video Shifter.

5. Wavering display, horizontal lines not occurring in the same place every time. The processor may be getting extra interrupts (if the processor is required to handle additional interrupts, it will not have timer to change all 16 color registers during a horizontal scan time). Examine the MFP interrupt request (pin 32). There should be an interrupt every 126 microseconds (2 display lines) from Display Enable (pin 20). If additional interrupts occur, locate the source: the inputs at pins 22-29 should all be high. If no external (to the MFP) source for the interrupts is found, replace the MFP.

   NOTE: if the keyboard is not connected, the input to the 6850 will be low, causing continual interrupts.

KEYBOARD TEST

Two types of test are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. If multiple tests have been selected, only the self-test is run. The operator presses keys and observes that the corresponding character on the screen changes (reverses background color). The key will also be displayed in the lower half of the screen. The mouse buttons and four directions are also shown on the screen. Connect the mouse and move in any direction and the arrow will flicker. Any key clicks while the mouse is moving indicates a short.

The self-test checks communication between the CPU and the keyboard microcomputer, and checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

KEYBOARD ERROR CODES

K0--Stuck key. A key closure was detected while the keyboard self test was executing.

K1--Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time. The keyboard needs to be replaced or the communication channel through the 6850 is not functional.

K2--Keyboard status error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status. Replace the keyboard.

MIDI TESTS

This test sends data out the MIDI port, (data loops back through the cable) and reads from the input and verifies the data is correct. This also tests the interrupt from the 6850 through the MFP chip. The LED in the loopback cable will blink as data is sent (not all cables have the LED).

MIDI ERROR CODES

M0--Data not received. Trace the signal from the output of the 6850, through the drivers, loopback cable, and receivers to the input of the 6850. Replace the defective component.

M1--Write/Read data mismatch. The data written was not the same as the data read. Replace 6850.

M2--Input frame error. Bad 6850 or bad driver or receiver causing noisy signal.

M3--Input parity error. Bad 6850 or bad driver or receiver causing noisy signal.

M4--Input data overrun. The 6850 received a byte before the previous byte was read. Probable bad 6850, also can be caused by the MFP not responding to the interrupt request.

RS232 TESTS

First the RS232 control lines are tested (which are tied together by the loopback connector), then the data loopback is tested. Data is checked transmissing?receiving using a polling method first, then using interrupts.

Data is transmitted at 300, 600, 1200...19200 bps. Data transmission is performed by the MFP and the 1488 and 1489 driver and receiver chips. Interrupts are a function of the MFP. Control lines are output by the PSG chip and input on the MFP. Note that this test does not thoroughly test the drive capability of the port, as the RS232 device may require voltage swings of 12 volts & there are no load resisters in the serial port diagnostic connector. If the test passes, but the unit fails in use, it is likely that the 1488 or 1489 chips are bad.

RS232 ERROR CODES

Data transmission error:

S0--Data not received. Check signal path: MFP pin 8 to J6 pin 2 via 1488 to J6 pin 3 to MFP pin 9 via 1489.

S1--Data mismatch. Data read was not what was sent. Check integrity of the signal. May be bad driver, receiver, or MFP.

S2--Input frame error. Incorrect time between start and stop bits. Probable MFP failure.

S3--Input parity error. Input data had incorrect parity. Probable MFP failure.

S4--Input data overrun. A byte was received before the CPU read the previous byte. MFP failure or, less likely, Glue failure.

S5--No IRQ. CPU did not detect an interrupt by the MFP. MFP or Glue failure.

S6--Transmit error. MFP transmitter failed.

S7--Transmit error interrupt. An error condition was created intentionally to cause an interrupt, and MFP didn't respond.

S8--Receive error interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.

S9--RI/DTR connection. Signal sent at DTR is not detected at RI.

SA--DCD/DTR connection. Signal sent at DTR is not detected at DCD.

SB--RTS/CTS connection. Signal sent at RTS is not detected at CTS.

AUDIO TEST

Outputs a low to high sweep on each of the three sound channels. One cycle of each channel is performed. If a channel is missing, replace the PSG chip. If no sound is heard, verify the output of the chip with an oscilloscope, and trace the signal to the monitor output connector. If no output from the PSG, verify the PSG is being selected by running the printer port or RS232 test (these tests both select the PSG).

TIMING TESTS

These tests are run at power-up as well as being selectable from the menu. The MFP timers, the Glue timing for VSYNC and HSYNC, and the Memory Controller video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as this test is run. There are two tests which check the bus timing for the 1772 and PSG chips. An error message is printed to the screen, then the test is run. If the test passes, the message is erased. If not, a Bus Error will occur and the message will remain. If a terminal is connected to the RS232 port, the message will not be erased, but "Pass" will be printed.

TIMING TEST ERROR CODES

T0--MFP timer error. One or more of the four timers in the MFP did not generate an interrupt on counting down .

T1--Vertical Sync. Glue is not generating vertical sync in the required time period.

T2--Horizontal Sync. Glue is not generating horizontal sync in the required time period.

T3--Display Enable. Glue is not generating DE output or the MFP is not generating an interrupt.

T4--Video Counter Error. The memory controller is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes. — (MMU)

T5--PSG Bus Error. The PSG chip is defective.

T6--1772 Bus Error. The 1772 chip is defective.

DMA TESTS

Four sectors (2048 bytes) of data are written to the RAM on the port test fixture via high speed DMA, then read back and verified. This test is repeated many times for RAM addresses throughout the range of RAM.

DMA TEST ERROR CODES

D0--DMA timed out. No DMA occurred due to faulty DMA Controller, Glue, or Memory Controller, or the HDINT interrupt was not processed by the MFP. The failure can be isolated by seeing if the DMA Controller responds to HDRQ from the test fixture with ACK. Verify the MFP by seeing that the HDINT input causes an INTR output from the MFP.

D1--DMA counter error. the number of bytes transferred was incorrect. The Memory Controller or DMA Controller is bad.

D2--Data mismatch error. The data received from the DMA port was not the same as the data sent. Replace the DMA Controller. If the problem persists, check the data lines to the port for opens and shorts. A third possibility is that a defective 1772 is loading the bus.

D3--DMA not responding. DMA controller could not respond to a data resquest from the external controller. Replace the DMA chip.

FLOPPY DISK TESTS

The Floppy Main Menu

```
Floppy disk drive routine
(WARNING -- all choices except 2,6,7 write to the disk)
1) Quick Test
2) Read Alignment Disk
3) Disk Interchange Test
4) Disk Exerciser
5) Check copy protect tracks (80-82)
6) Test Speed
7) Install disk drives
```

In single test mode, a menu is displayed showing seven options:

1. Quick test. For each disk installed, formats, writes, and reads tracks 0, 1, and 79 of side 0. If double sided, formats and writes track 79 of side 1 and verifies that side 0 was not overwritten. If no disks are installed, checks to see what drives are online and if they are double or single sided. To assure that the drive are correctly tested, the operator should install (menu option 6) before calling the test. Once the test is run, the drives become installed, and will be displayed on the menu screen (below the RAM size).

2. Read track. Continuously reads a track, for checking alignment with an analog alignment diskette. The track to be read may be input by the operator. If "Return" is pressed without entering a number, the default is track 40.

3. Interchangeability test. Checks to see if diskettes from two disk drives each can be read by the other disk drive.

4. Disk exerciser. A more thorough disk test; tests all sectors on the disk for an indefinite period of time.

5. Copy Protect Tracks. Tests tracks 80-82, which are used by some software companies for copy protection). Not all failures are cause for replacement because some manufacturers disk drives will not write to these tracks.

6. Test speed. The rotational speed of the drive is tested and displayed on the screen as the period of rotation. The acceptable range is 196-204 milliseconds. The highest and lowest values measured are displayed. The test stops when any key is pressed.

7. Install disks. Specify how many and what type of disks to test.

If more than one test is selected from the main menu, the floppy menu will not appear, but the Quick Test will be selected automatically.

FLOPPY TEST ERROR CODES

No floppies connected--the controller cannot read index pulses. The cable may be improperly connected, or the drive has no power, or the drive is faulty.

F0--Drive not selected. Drive was installed, but failed attempting restore (seek to track 0). Check connection of cables, power to drive. Verify the light on the front of the drive goes on. Listen for the sound of the head seeking (the slide on the diskette should open). If all this occurs, TR0 (pin 23 on the 1772) should go low. If so, check for an interrupt on pin 28 of the 1772. If none, replace the 1772. Else trace the interrupt to the MFP, verify that the MFP responds be asserting INTR. If the drive is not being selected (no light), check the PSG chip. Pin 20 should go low when drive A is selected, and pin 19 should go low when drive B is selected. If not, replace the PSG.

F1,F2,F3 errors of previous versions have been deleted. The error message now says "Error Writing" (or reading or formatting), and displays a more specific error message, e.g., "F9 CRC error".

F4--Seek error. Verify that the STEP, MO, and DIRC outputs from the 1772 are sent to the drive. Probable failure in the 1772, but the drive is also suspect.

F5--Write protected. Check the write protect tab on the diskette. If OK, verify that the WP input (1772 pin 25) is going low during the test; if it is, then the 1772 is defective; if not, the problem is with the disk drive.

F6--Read compare error. Data read from the disk was not what was supposed to be written. Check in the following order: diskette, disk drive, 1772, and DMA Controller.

F7--DMA error. DMA Controller could not respond to a request for DMA. Replace the DMA Controller. If error persists, check FDRQ while running the test. It should normally be low and go high with each data byte transferred. If stuck high, push the reset button and verify that MR (1772 pin 13) goes low. If not, trace RESET to its source. If MR is OK, but FDRQ is still stuck, replace the 1772.

F8--DMA count error. Replace the Memory Controller, if that does not fix it, replace the DMA Controller.

F9--CRC error. The diskette or disk drive may be bad, else replace the 1772.

FA--Record not found. The 1772 could not read a sector header. May be a bad diskette, drive or 1772. If the test fails drive A but not drive B, the 1772 is not at fault (likewise fails B not A).

FB--Lost data. Data was transferred to the 1772 faster than the 1772 could transfer to the DMA Controller. If DMA Port test passes, the 1772 is probably bad. The DMA Controller could also be at fault.

FC--Side select error--single sided drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.

FD--Drive not ready. The format/write/read operation timed-out. Probably a bad disk drive. Verify by checking another drive. Could also be a faulty 1772.

Soft Error = does not cause a failure after 1 retry. (If doesn't fail a second time.)

Hard Error = failed second retry. Unit will halt if you reach any of the following: 20 read errors, 20 write errors or 5 format errors.

PRINTER AND JOYSTICK PORT TESTS

The port test fixture is used to test the parallel printer port and joystick ports. The parallel port test writes to a latch on the test fixture and reads back data. The joystick port test outputs data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU. The cables connecting the joystick ports to the test fixture must not be reversed, or the printer and joystick tests will fail.

PRINTER/JOYSTICK ERROR CODES

P0--Printer port error. Data read from the printer port was not what was written. Verify that the data lines on the PSG chip (pins 6-13) are toggling when the test is run. If not, run the RS232 test. If the RI-DTR and DCD-DTR errors occur, the chip is probably not being selected. Check if the chip selects are being activated and the 2MHz clock is present. If the PSG is selected and not outputting signals, replace it. If the data lines toggle, verify continuity. Also verify that J11 (Joystick 0) pin 3 is pulled up. Verify the test fixture is good by testing another computer. If it is OK, replace the PSG.

P1--Busy input error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected. If the P0 error also occurs, see handling for that. Otherwise, look for a signal arriving at MFP pin 22 from J5 pin 11. If no signal at J5, the test fixture may be bad. Verify with another computer.

J0--Joystick Port 0. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 12,10,9,8 respectively.

J1--Joystick Port 1. The keyboard input is not functioning. If the Busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 pins 1,2,3,4 to J12 pins 7,5,4,3 respectively.

J2--Joystick time-out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, keyboard-CPU communication line, or a faulty test fixture. If the power-up keyboard test passes, this eliminates any problem with keyboard-CPU communication.

J3--Left button input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, also check continuity from J10 pin 6 to J12 pin 11.

J4--Right button input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the 520ST, also check continuity from J10 pin 6 to J12 pin 6.

HIGH RESOLUTION MONITOR

If this test is selected while a color monitor is connected, a message is displayed to connect the monochrome monitor. The CPU waits for an interrupt from the MONOMON input to the MFP, and when received (the operator connects the monochrome monitor), changes the display to high resolution. The display screen shows horizontal and vertical lines, each 2 pixels in width. The screen will reverse every two seconds. When the operator sees the display is correct, he unplugs the monochrome monitor and re-connects the RGB monitor and the display should return to normal.

GRAPHICS CHIP (BLiTTER)

This tests the ability of the BITBLiT to move blocks of memory around and perform logical operations on the data. No patterns appear on the screen. Many different error messages are possible (G0-G13), but the action for any error is the same: replace the chip. A faulty BLiTTER may cause a BUS ERROR.

REAL-TIME CLOCK

The test saves the current time and date, and writes a new time, waits one second, and verifies that hours, minutes, seconds, etc. have all rolled over. The is repeated for another date to verify all registers.

EXPANSION CONNECTOR

This test, for Mega models, requires the expansion test fixture (the top cover and shield must be removed to install the test fixture). It tests the expansion interface, in part by software, and the remainder by LEDs. The data and address busses and interrupt lines are tested in software. The control lines from the CPU are tested with the LEDs. Most of the LEDs will go off after the system is turned on and the menu appears on the screen. Three LEDs will remain lit: BR (bus request), BG (bus grant) and BGACK (bus grant acknowledge). These should go off after (1) the expansion connector test is run and (2) either the DMA test or floppy test are run. The LEDs simply indicate that the line is toggling. A lit LED means the line is not changing.

The software tests three groups of signals: data bus, address bus, and interrupts.

The first test writes and reads the RAM on the test fixture, setting one bit high at a time, to check for open or shorted data lines. If an error is found, the message "EX0 bad bit" is displayed.

The second test writes an incrementing pattern (0,1,2,...) across address bits 0-15, then across address bits 16-23 to the RAM on the test fixture to check for open or shorted address bits. If an error is found, the message "EX1 external RAM error, low byte" or "EX2 external RAM error, high byte" is printed, depending on whether the error occurred in the low or high address.

The third test uses circuitry on the external test fixture to create interrupt requests. There are three interrupts: INT3, INT5, and INT7. If the appropriate interrupt does not occur when expected, then a message is displayed: "EX3 INT3 error, "EX4 INT5 error", or "EX5 INT7 error".

ERROR CODES QUICK REFERENCE

This is a brief summary of all error code which may occur when running the diagnostic.

INITIALIZATION (Errors occurring before the title and menu appear)

I1 RAM data line is stuck.
I2 RAM disturbance. Location is altered by write to another location.
I3 RAM addressing. Wrong location is being addressed.
I4 MMU error. No DTACK after RAM access.
I5 RAM sizing error. Uppermost address fails.
I6

EXCEPTIONS (may occur at any time)

E1--E5 not used
E6 Autovector error. IPL0 is grounded or 68000 is bad.
E7 Spurious interrupt. Bus error during exception processing. Device interrupted, but did not provide interrupt vector.
E8 Internal Exception (generated by 68000).
E9 Bad Instruction Fetch.
EA Address error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceded by a bus error or bad instruction fetch.
EB Bus error. Generated internally by the 68000 or externally by Glue. Usually caused by device not responding. Displays the address of the device being accessed.

RAM

R0 Error in low memory (first 2K), possibly affecting program execution.
R1 Error in RAM chip.
R2 Address error. Bad RAM chip or memory controller. Address line not working.
R3 Address error at 64k boundary.
R4 Error during video RAM test. Bad RAM chip.

KEYBOARD

K0 Stuck key
K1 Keyboard controller is not responding.
K2 Keyboard controller reports error.

MIDI

M0 Data not received.
M1 Data received is not what was sent.
M2 Data input framing error.
M3 Parity error.
M4 Data overrun. Byte was not read from the 6850 before next byte arrived.

RS232

S0 Data not received.
S1 Data received is not what was sent.
S2 Data input framing error.
S3 Parity error.
S4 Data overrun. Byte was not read from the MFP before the next byte arrived.
S5 IRQ. The MFP is not generating interrupts for transmit or receive.
S6 Transmitter error--MFP.
S7 No interrupt from transmit error (MFP).
S8 No interrupt from receive error (MFP).
S9 DTR--RI. These signals are connected by the loopback connector. Changing DTR does not cause change in RI.
SA DTR--DCD. Same as S9 for these signals.
SB RTS--CTS. Same as S9 for these signals.

DMA

D0 Time-out. DMA did not take place, or interrupt not detected.
D1 DMA count error. Not all bytes arrived. Possible Memory Controller error.
D3 DMA Controller not responding.

TIMING

T0 MFP timers failed.
T1 Vertical sync timing failed.
T2 Horizontal sync timing failed.
T3 Display Enable Interrupt failed.
T4 Memory Controller video address counter failed. (Vain 68000).
T5 PSG Bus test. PSG chip is causing a bus error by staying on the data bus too long.
T6 1772 Bus test. 1772 chip is causing a bus error by staying on the data bus too long.

PRINTER AND JOYSTICK PORTS

P0 Printer port error.
P1 Busy (printer port input) failed.
J0 Joystick port 0 failed.
J1 Joystick port 1 failed.
J2 Joystick (keyboard controller) timed-out.
J3 Left button line failed.
J4 Right button line failed.

FLOPPY DISK DRIVE

F0 Drive offline. Not responding to restore (seek track 0).
F1 Format error.

(Note: former F2,F3 write and read errors are deleted. The message now will say "error writing" [or reading] and display the specific error found.)

F4 Seek error.
F5 Write protected.
F6 Data compare. (Data read not equal to data written.)
F7 DMA error.
F8 DMA count error (Memory Controller counter.)
F9 CRC error.
FA Record not found.
FB Lost data.
FC Side select error.
FD Drive not ready. Timed-out performing the command.

SECTION FOUR
DISASSEMBLY/ASSEMBLY

MEGA/ST DISASSEMBLY

Top Cover Removal:

1) Remove keyboard connector from the side of the top cover.

2) Turn unit upside down.

3) Remove the 9 screws from the square holes. These fasten the top case to the bottom. If the printed circuit board is to be exposed, or the disk drive is to be removed, also remove the three screws from the round holes. These hold the disk drive in place.

4) Turn the unit upright. While lifting the top cover up slightly from the back, unplug the battery connector from underneat its left rear corner. Now the cover can be removed easily.

Upper Shield Removal:

1) Straighten the six twist tabs. Note that there is one located under the disk drive.

2) Lift the shield up from the back gentlely so that it will be free from anythings in the rear.

3) Push the disk drive up while lifting up the front of top shield out of the bottom cover and pull forward.

Disk Drive Removal:

1) Lift the disk drive slightly and unplug the power harness connector and the ribbon cable.

Power Supply Removal:

1) Remove the 2 screws at front corners of power supply.

2) Unplug the wire harness connector in the right front corner of the power supply.

3) Lift the power supply up out of the main assembly.

Removal of main assembly from bottom case:

1) If power supply has not already been removed, then follow the power supply removal section to remove it.

2) Remove the six studs which secure the I/O shield to the bottom case.

3) Lift the assembly up from the front and pull forward.

Removal of Shield From Printed Circuit Board:

1) Straighten six twist tabs. It may be necessary to pull the twist tabs away from the board slightly.

2) Remove the I/O shield in the back.

   Note: Now that the major components are exposed, this is a convenient configuration for troubleshooting. The keyboard and disk drive may be re-connected and placed off to the side if those components are needed.

3) Lift the printed circuit assembly away from bottom shield.

Mega/ST RE-ASSEMBLY

1) Place insulation panel on bottom shield.

2) Attach the I/O shield to the I/O ports. Place Main Board on top of Bottom Shield over insulator panel.

3) Place the assembly in lower plastic case.

4) Secure the I/O shield to the bottom case with the 6 studs.

5) Plug in power supply connector and position power supply with tabs in slots.

6) Place assembly in lower plastic case.

7) Fasten the power supply to the bottom case at both front corners with two screws. This can be done with the power supply shield in place, using a magnestized screwdriver to hold the screw, or by removing the shield.

8) Plug disk drive power and ribbon cables into drive (cables go under shield), and position drive over standoffs.

9) Push the battery connector up from the opening located in the left rear corner of the top shield.

10) Align tabs on bottom shield with slots on top shield and fit top shield over main assembly. Twist the tabs to lock in place.

11) Place the top cover over the assembly.

12) Turn over the assembly and replace the 9 screws. The three longer screws go into the round holes to secure the disk drive.

A WORD OF CAUTION

It is strongly recommended that the computer be retested once in plastic to make sure that the re-assembly was done correctly and there are no shorts to Shield.

SECTION FIVE
SYMPTOM CHECKLIST

This section gives a brief summary of common problems and their most probable causes. For more detail, refer to the section on troubleshooting in this document, or the Diagnostic Cartridge Troubleshooting Guide.

Symptom	Probable Cause
DISPLAY PROBLEMS	
Black screen	No power (check LED), bad Glue chip, bad Video Shifter. See TESTING section, "Troubleshooting a Dead Unit".
White screen	Video Shifter, Glue, Memory Controller, DMA Controller, 68000. Use diagnostic cartridge with terminal connected via RS232 port.
Dots/bars on screen	RAM, Memory Controller, Video Shifter. Use diagnostic cartridge.
One color missing	video summer, buffer, Video Shifter. Check signals with oscilloscope.
Scrambled screen	Glue, Memory Controller. Use the diagnostic cartridge.
T.V. output bad	Modulator, phase locked loop. Trace the signal with your oscilloscope.
DISK DRIVE PROBLEMS	
Disk won't boot	Power supply, FDC (1772), DMA Controller, PSG chip, disk drive. See if select light goes on, if not, check PSG outputs. Listen for motor spinning. If not, check the power supply. Swap disk drive or try an external drive. If not working, check DMA Controller and 1772 with the diagnostic cart.
Disk won't format	FDC(1772), DMA Controller, disk drive.
System crash after loading files	Diskette, disk drive, FDC (1772), DMA, or Memory Controller. Swap diskette, retry. Use the diagnostics to check FDC (1772), DMA Controller, Memory Controller; or replace disk drive.

Systoms	Probable Cause
KEYBOARD PROBLEMS	
Keys won't work	Bad keyboard controller, 6850, MFP.
Keys won't work but mouse does	Keyboard cable was inserted while unit was powered, recycle power.
MIDI PROBLEMS	
No data	Bad opto-isolator chip, 6850, inverter (74LS04 , 74LS05).
RS232 PROBLEMS	
No data	Bad 68901 MFP, receiver, driver, or PSG chips, +/- 12v supply is blown. Use diagnostics to isolate bad line(s).
PRINTER PORT PROBLEMS	
No output	Bad PSG, MFP chips.
Does not output to a specific printer	Input impedance of printer is less than 3K ohm ,modify pullup resistors on printer.
DMA PORT PROBLEMS	
Does not function	Bad DMA Controller, Memory Controller, 1772 (loading the bus).
REAL TIME CLOCK PROBLEMS	
Does not function	Bad RTC PAL chip, clock chip, crystal.
Does not save time after cold boot	Bad batteries, power off sense circuit.
BLiTTER PROBLEMS	
No video when Blit is inserted	Jumpers below and to right of blitter chip must be cut before blitter will work.
Does not function	Replace blitter chip if above step doesn't fix problem.

SECTION SIX
DIAGNOSTIC FLOWCHARTS

This section summarizes in diagramatic form the steps taken in troubleshooting the Mega using the diagnostic cartridge. The details of using the cartridge are not shown; this shows the context in which the cartridge would be used, including some problems for which the cartridge would not be useful. Usage of the cartridge is covered in the troubleshooting guide. In general, the user would run all the tests, look up errors in the troubleshooting guide, and take the action recommended.

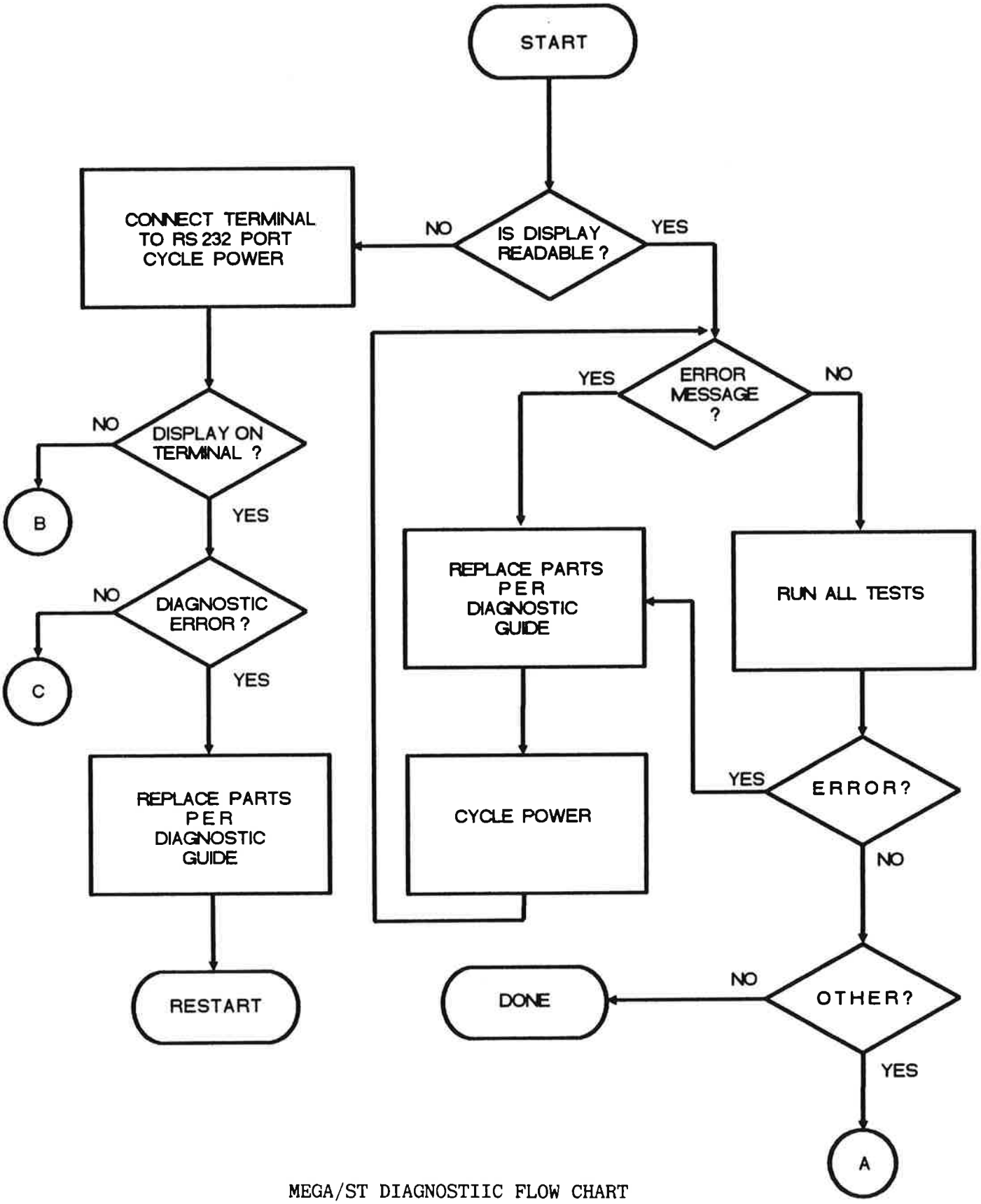
Although a thorough understanding of the system may be necessary in solving some problems, in most cases following the flowchart, reading the documentation on the diagnostic cartridge where necessary, and swapping out the indicated components will result in repair of the problem.

Replacement Procedures

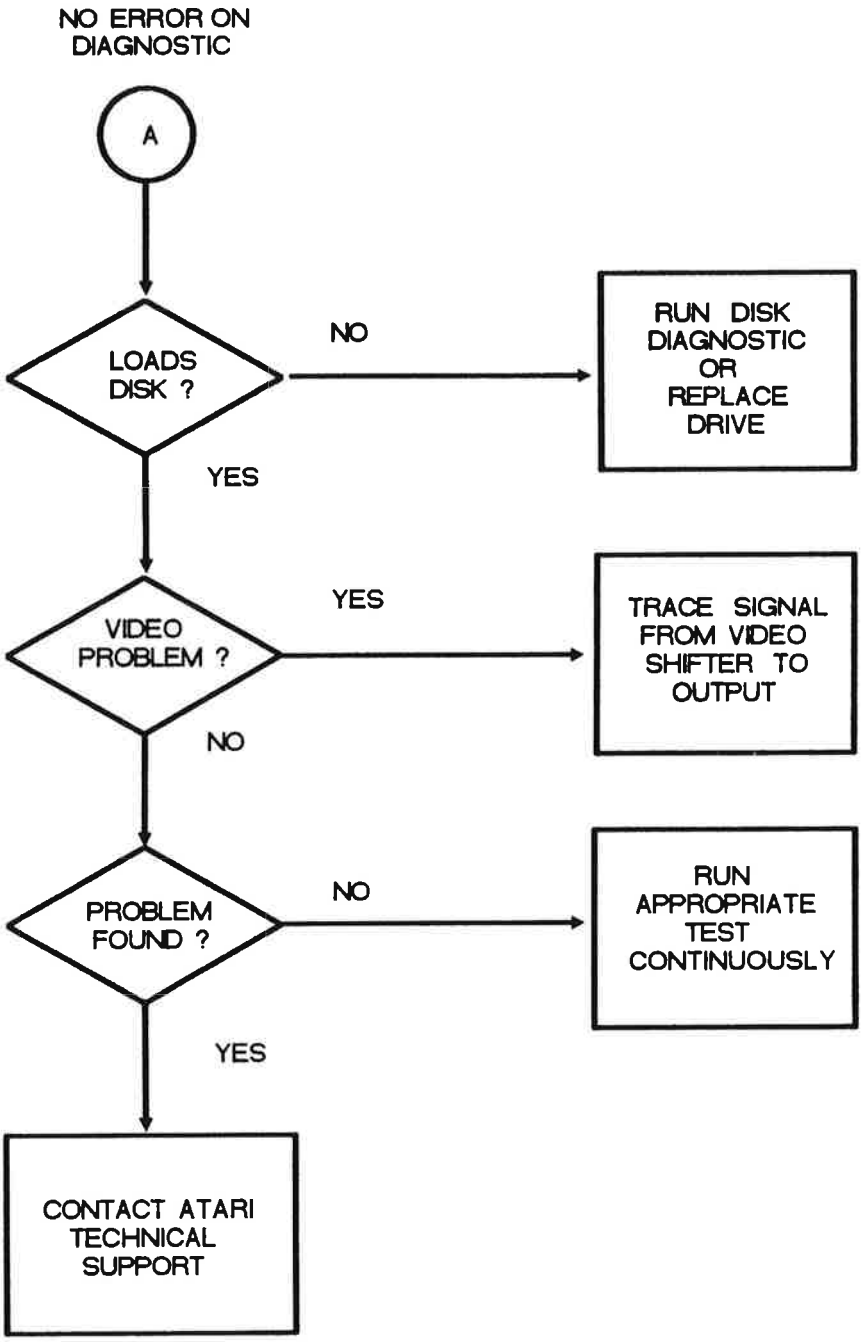
Where replacement is indicated, replace the component (if more than one is indicated, replace one at a time) with a known good part. If other components are later replaced, verify whether the first part is good by replacing in the system once the system has been repaired.

Handling of Integrated Circuits

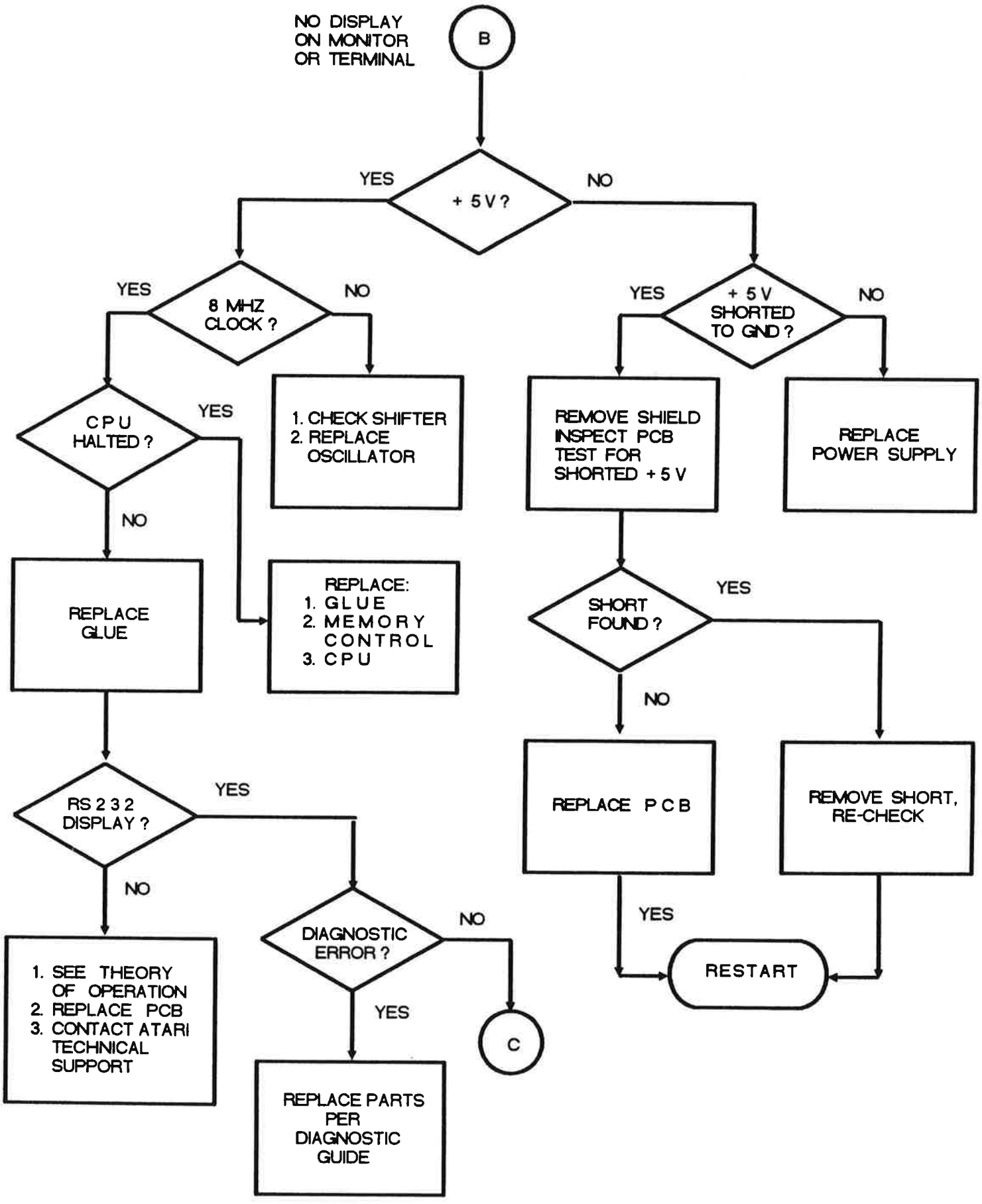
Extreme care should be taken when handling the integrated circuit chips. They are very sensitive to static electricity and can easily be damaged by careless handling. Keep chips in their plastic carriers or on conductive foam when not in use.

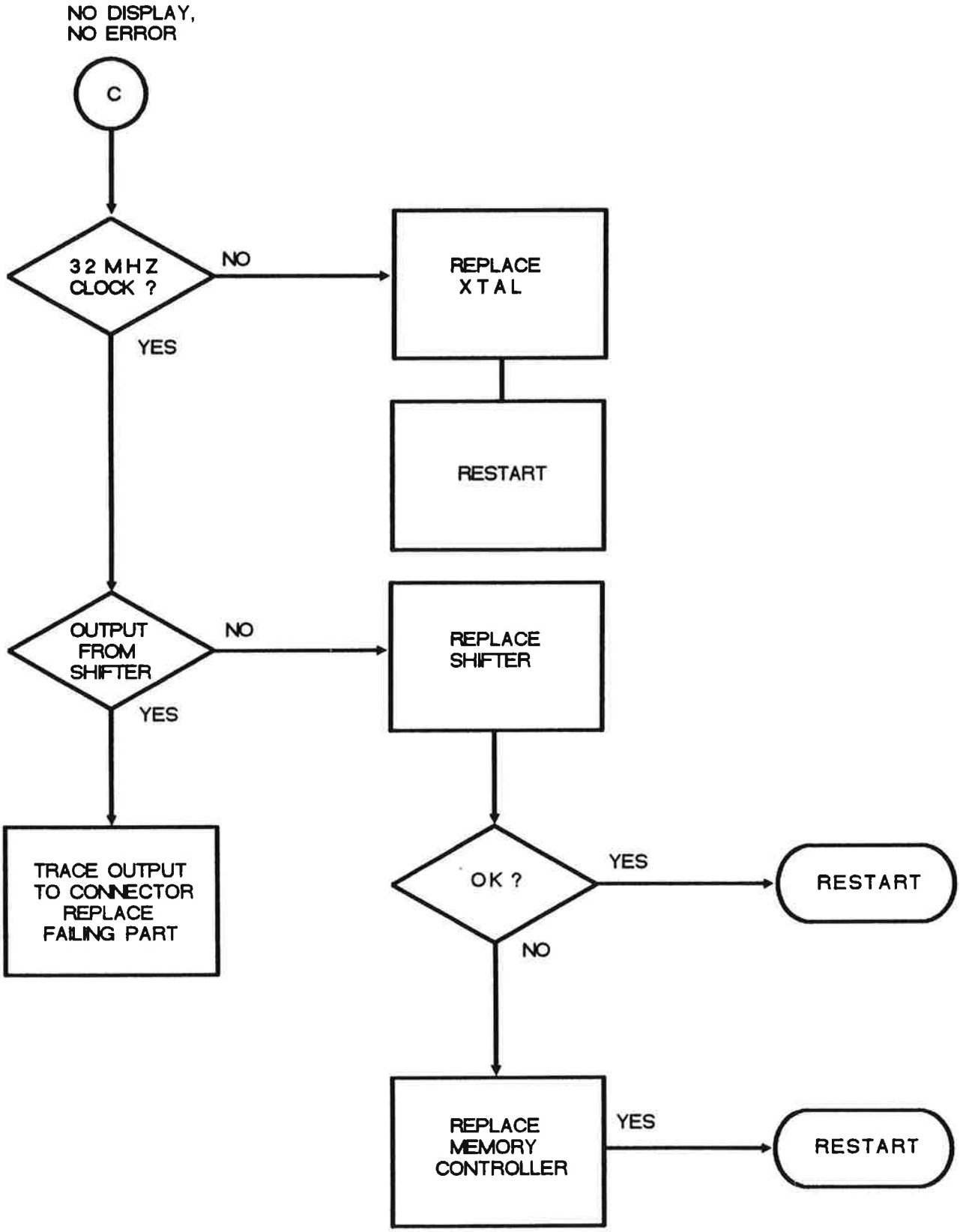


MEGA/ST DIAGNOSTIIC FLOW CHART



MEGA/ST DIAGNOSTIIC FLOW CHART


NO DISPLAY ON MONITOR OR TERMINAL
B
+ 5 V ?
YES
NO
8 MHZ CLOCK ?
YES
NO
1. CHECK SHIFTER
2. REPLACE OSCILLATOR
CPU HALTED ?
YES
NO
REPLACE GLUE
REPLACE:
1. GLUE
2. MEMORY CONTROL
3. CPU
RS 232 DISPLAY ?
YES
NO
1. SEE THEORY OF OPERATION
2. REPLACE PCB
3. CONTACT ATARI TECHNICAL SUPPORT
DIAGNOSTIC ERROR ?
NO
YES
C
REPLACE PARTS PER DIAGNOSTIC GUIDE
+ 5 V SHORTED TO GND ?
YES
NO
REMOVE SHIELD INSPECT PCB TEST FOR SHORTED + 5 V
REPLACE POWER SUPPLY
SHORT FOUND ?
YES
NO
REPLACE PCB
REMOVE SHORT, RE-CHECK
YES
RESTART



MEGA/ST DIAGNOSTIIC FLOW CHART

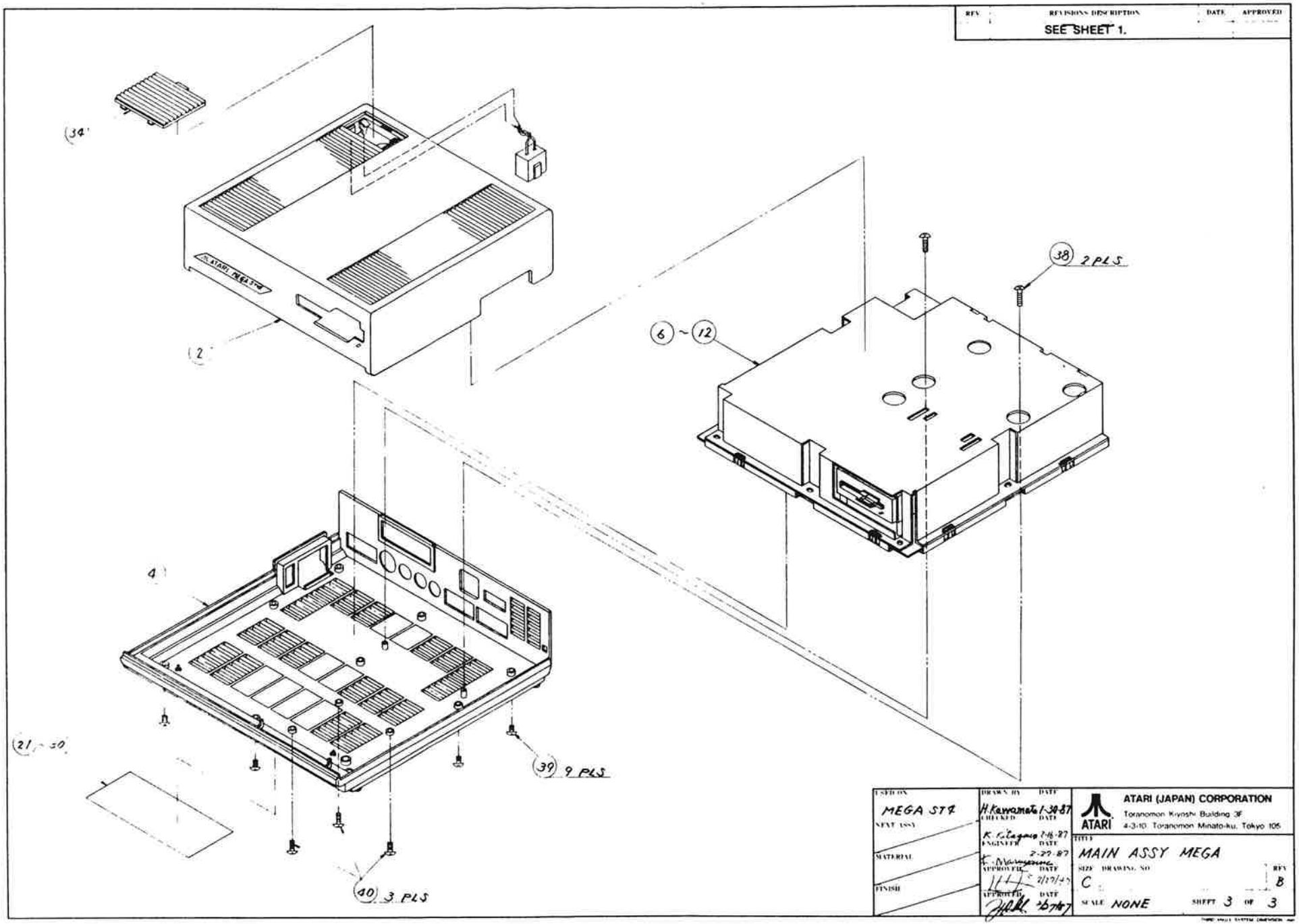
SECTION SEVEN
PARTS LISTS AND ASSEMBLY DRAWINGS

MEGA PARTS LIST

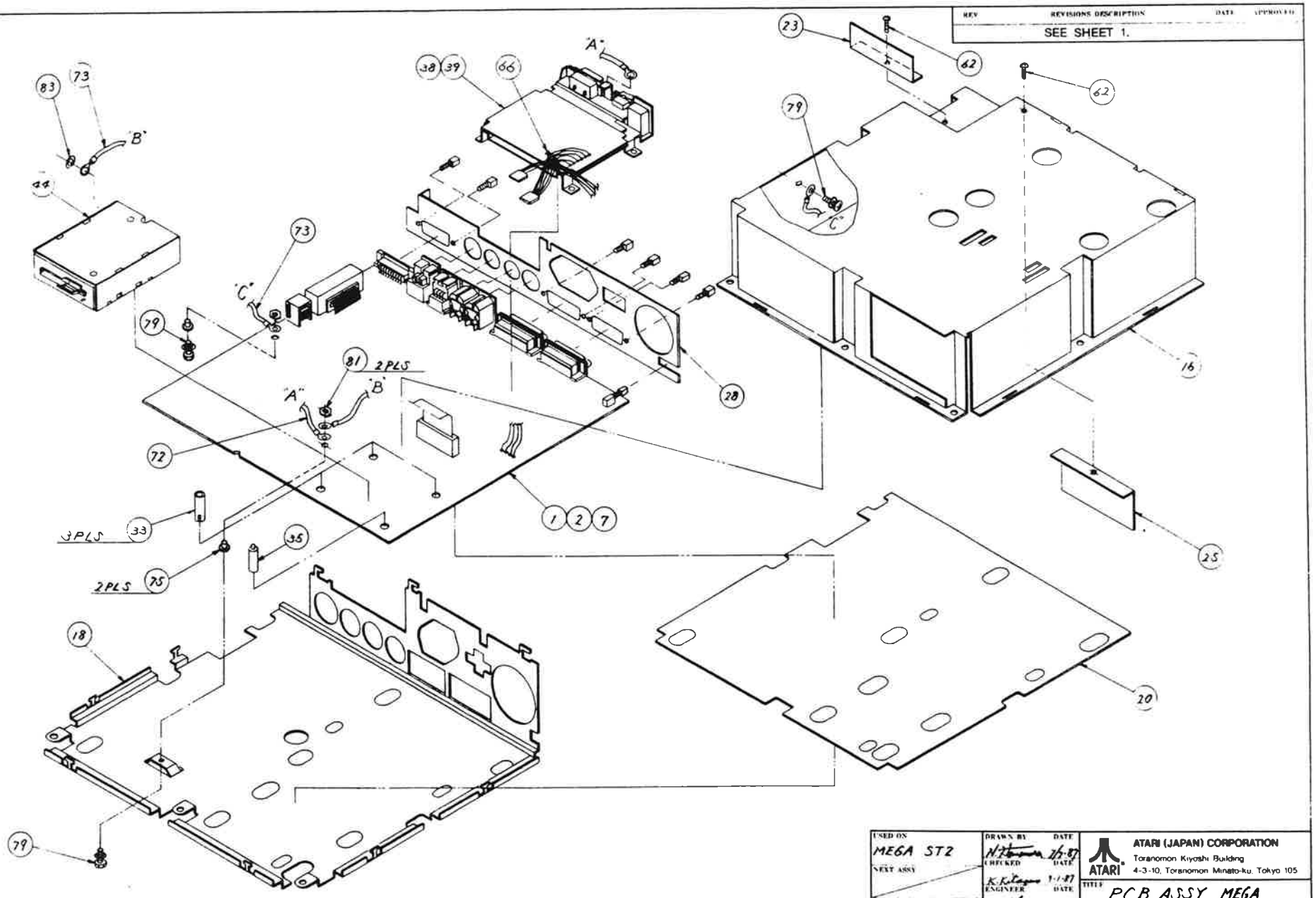
PART NUMBER	DESCRIPTION	LOCATION
CA200055-001	PCBA (1MB ROM) MEGA 4	SUBASSEMBLY
CA200093-001	PCBA (1MB ROM) MEGA 2	SUBASSEMBLY
CA200008-001	MEGA POWER SUPPLY w/FAN	SUBASSEMBLY
CA200018-001	MEGA 2/4 CASE BOTTOM	SUBASSEMBLY
CA200022-001	MEGA 2 CASE TOP	SUBASSEMBLY
CA200025-001	MEGA 4 CASE TOP	SUBASSEMBLY
CA200039-001	MEGA KEYBOARD COMPLETE	SUBASSEMBLY
CA200040-001	MEGA KEYBOARD CASE TOP	SUBASSEMBLY
CA200041-001	MEGA KEYBOARD CASE BOTTOM	SUBASSEMBLY
CA200042-001	MEGA KEYBOARD CONNECTOR PCBA	SUBASSEMBLY
CA200043-001	MEGA KEYBOARD (ONLY)	SUBASSEMBLY
CA200054-001	MEGA KEYBOARD CABLE	SUBASSEMBLY
C070350-003	FDD UNIT (1M BYTE) NEWTRONICS	SUBASSEMBLY
C070352-003	FDD UNIT (IM BYTE) CHINON	SUB FOR ABOVE
C103047-001	FDD UNIT (IM BYTE) CHINON	SUB FOR ABOVE
CA070025	STM1 MOUSE ASSEMBLY	ASSEMBLY
	CAP 30pF 50V ±5% CH. CER AXIAL	C39,40
	CAP 39pF 50V ±5% CH. CER AXIAL	C54
	CAP 100pF 50V ±5% SL. CER AXIAL	C43~46
	CAP 150pF 50V ±5% CH. CER AXIAL	C28
	CAP 330pF 50V ±10% B. CER AXIAL	C29
	CAP 1000pF 25V ±20% X. CER AXIAL	C68,69
	CAP 0.1µF 25VZ. CER AXIAL	C1,2,5~7,9~21,23,26 27,30~33,36,38,41, 42,47,48,50,52,55, 56,57,59,60,64~66, 70,73,112,113,120, 121~123
	CAP 0.22µF 50V Z5U. CER AXIAL	C80~95
	CAP 0.47µF 25V Z.CER AXIAL	C67
	CAP 4.7µF 25V ELEC AXIAL	C22,24,25
	CAP 10µF 16V ELEC AXIAL	C3
	CAP 47µF 16V ELEC RADIAL	C34,35
	CAP 100µF 16V ELEC AXIAL	C8,37,51
	CAP 1000µF 16V ELEC AXIAL	C140
	CAP 4700µF 16V ELEC RADIAL	C4
	CAP 1001µF 16V ELEC RADIAL	C49
	CAP 5-30pF TRIMMER	C53
	RES 0 OHM JUMPER	R120,123,126,145, 146,D12~14,W2,3
	RES 5.1 OHM 1/4W 5% CARBON	R15
	RES 27 OHM 1/4W 5% CARBON	R83
	RES 33 OHM 1/4W 5% CARBON	R52,54,55,57,60~66 68,76,110,113
	RES 47 OHM 1/4W 5% CARBON	R45~48
	RES 75 OHM 1/4W 5% CARBON	R67,73,77
	RES 100 OHM 1/4W 5% CARBON	R69,75,78,86,116
	RES 150 OHM 1/4W 5% CARBON	R23,115
	RES 220 OHM 1/4W 5% CARBON	R10,14,16,17,19,44
	RES 470 OHM 1/4W 5% CARBON	R26
	RES 1K OHM 1/4W 5% CARBON	R1,2,4,21,24,30,37 38,40~43,82,85,111
	RES 1.2K OHM 1/4W 5% CARBON	R20,76

PART NUMBER	DESCRIPTION	LOCATION
	RES 2.2K OHM 1/4W 5% CARBON	R5
	RES 3.3K OHM 1/4W 5% CARBON	R27
	RES 4.7K OHM 1/4W 5% CARBON	R6,11,28,29,39,112
	RES 5.1K OHM 1/4W 5% CARBON	R22
	RES 10K OHM 1/4W 5% CARBON	R7,8,25,33~36,108, 109,114
	RES 12K OHM 1/4W 5% CARBON	R18
	RES 51K OHM 1/4W 5% CARBON	R32
C070567-004	RES NETWORK 1K OHM X 6	Rp7
C070159-006	RES NETWORK 4.7K OHM X 8	RP1~4
C070448	RES NETWORK 10K OHM X 8	RP5,6
C014384	INDUCTOR FERITE BEAD AXIAL	L1,12,45,46,48
C070205	INDUCTOR 0.27uH 20% AXIAL	L47
C070471-001	INDUCTOR 10μH 10% AXIAL	L50
C070471-002	INDUCTOR 220μH 10% AXIAL	L5
C070790	LINE FILTER	L9
C070241-002	NOISE FILTER ZJS5101-02	L2~4,6~8,13~22,24 ~30,32~43
	TRANSISTOR 2N3904	Q1,3,6~10
	TRANSISTOR 2N3906	Q2
	DIODE 1N914	D1~3,5~8,15~18
C101805	DIODE 1SS108 SCHOTTKY BARRIER	D4
C025993	CRYSTAL 2.4576 MHZ	Y1
C100232	CRYSTAL 32.768KHZ	Y2
C100281	CRYSTAL 32.0424 MHZ	OSC1
C070129	CONN 40 PIN RIGHT ANGLE	J2
C070130	CONN DB-19S HARD DISK	J10
C070131	CONN 14 PIN DIN FLOPPY DISK	J13
	CONN DB-25P RS232C	J7
	CONN DB-25S PARALELL	J6
C070134	CONN 13 PIN DIN VIDEO	J14
C070033	CONN 5 PIN DIN MIDI	J3,4
C070445	CONN SINGLE INLINE 6 PIN	J1,18
C070644-011	CONN DOUBLE INLINE 24 PIN	J17
C100283-001	CONN DOUBLE INLINE MALE 64 PIN	J15
	SOCKET 40 PIN	U27,31
	SOCKET 28 PIN	U3,4,6,7,9,10
C070120	SOCKET 68 PIN LCC	U5,17,30
C070119	PUSH SWITCH	S1
CA070024	FLAT CABLE 34P ASSEMBLED	J12
CA070023-003	CABLE 4P ASSEMBLED	J11
CA200053-002	CABLE ASSY:MALE TYPE 2 PIN	J9
C101643	IC CUSTOM ST BLITTER	U5
C025982	IC 68000-8 CPU	U8
C025913	IC CUSTOM DMA CONTROLLER	U27
C025915	IC CUSTOM GLUE	U17
C025914	IC CUSTOM SHIFTER	U31 or
C101608	IC CUSTOM FULL SHIFTER (w/D/A)	U31
C025912	IC CUSTOM MMU	U30
C025986	IC 1489 RS-232C, RECEIVER	U19
C025987	IC 1488 RS-232C, DRIVER	U20
C025983	IC YM2149, SOUND	U16
C025984	IC 68901, MFP	U18
C025985	IC 6850, ACIA	U14,15
C101712	IC DYNAMIC RAM 1M X 1	U40~55(60~75)
C025988	IC PC900 PHOTO COUPLER	U13

PART NUMBER	DESCRIPTION	LOCATION
C101621	IC TL 7705A	U1
	IC 74LS02, QUAD NOR	U21
	IC 74LS06, HEX INVERTER O.C.	U26
	IC 74LS07, HEX O.C. BUFFER	U2
	IC 74LS32, QUAD 2-INPUT OR GATE	U78
	IC 74LS148 8-3 PRIOR ENCODER	U39
	IC 74HC00 QUAD NAND GATE	U24
C101622	IC RP5C15 REAL TIME CLOCK	U25
C101625	IC RTCPAL PAL16L8	U37
	IC 74LS244.3 STATE LINE BUFFER	U32,35,58,59
	IC 74LS373 LATCH	U33,36
	IC 74LS11 TRIPLE 3-INPUT AND GATE	U12
C070447	IC TL497A SWITCHING REGULATOR	U22
C026028	IC WD-1772 FDD CONTROLLER	U28
C101629-001	IC; TOS ROM 1 MEG HI-0	U9
C101630-001	IC; TOS ROM 1 MEG LO-0	U10
C070349-002	AC POWER CORD (UL/CSA)	
C100296-001	MEGA MANUAL OWNERS	
C070322	COLLAR A	3 DRIVE SPACERS
C070323	COLLAR B	1 DRIVE SPACER

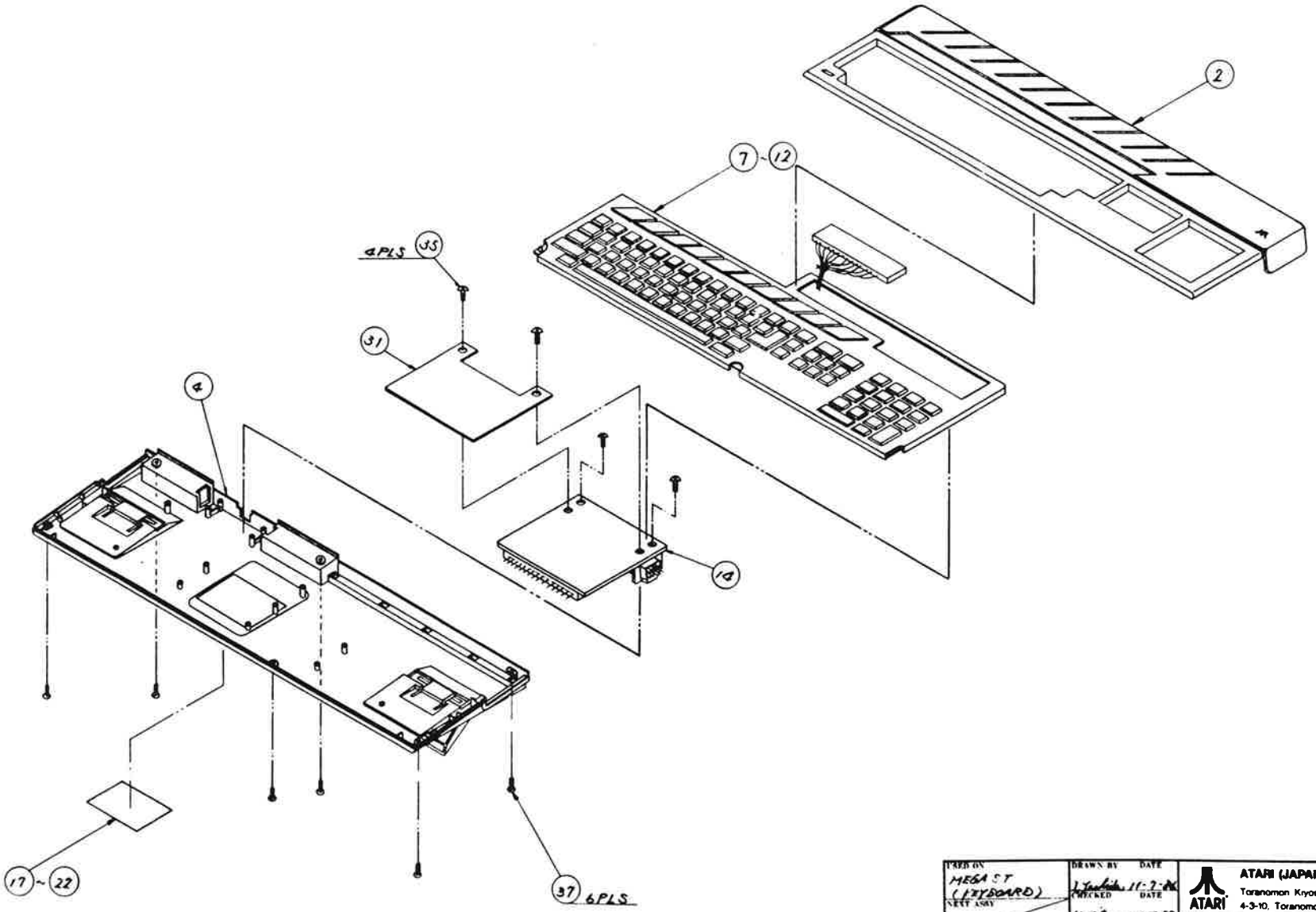

REV
REVISIONS DESCRIPTION
DATE
APPROVED
SEE SHEET 1.
(34)
(2)
(6) ~ (12)
(38) 2 PLS
(4)
(21) ~ (30)
(39) 9 PLS
(40) 3 PLS
DESCRIPTION
MEGA ST2
NEXT ASSY
MATERIAL
FINISH
DRAWN BY
H.Kawamoto 1-30-87
CHECKED
K.Kitagawa 2-16-87
ENGINEER
2-27-87
APPROVED
2/27/87
APPROVED BY
DATE
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10 Toranomon Minato-ku, Tokyo 105
TITLE
MAIN ASSY MEGA
SIZE
C
DRAWING NO
REV
B
SCALE NONE
SHEET 3 OF 3

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



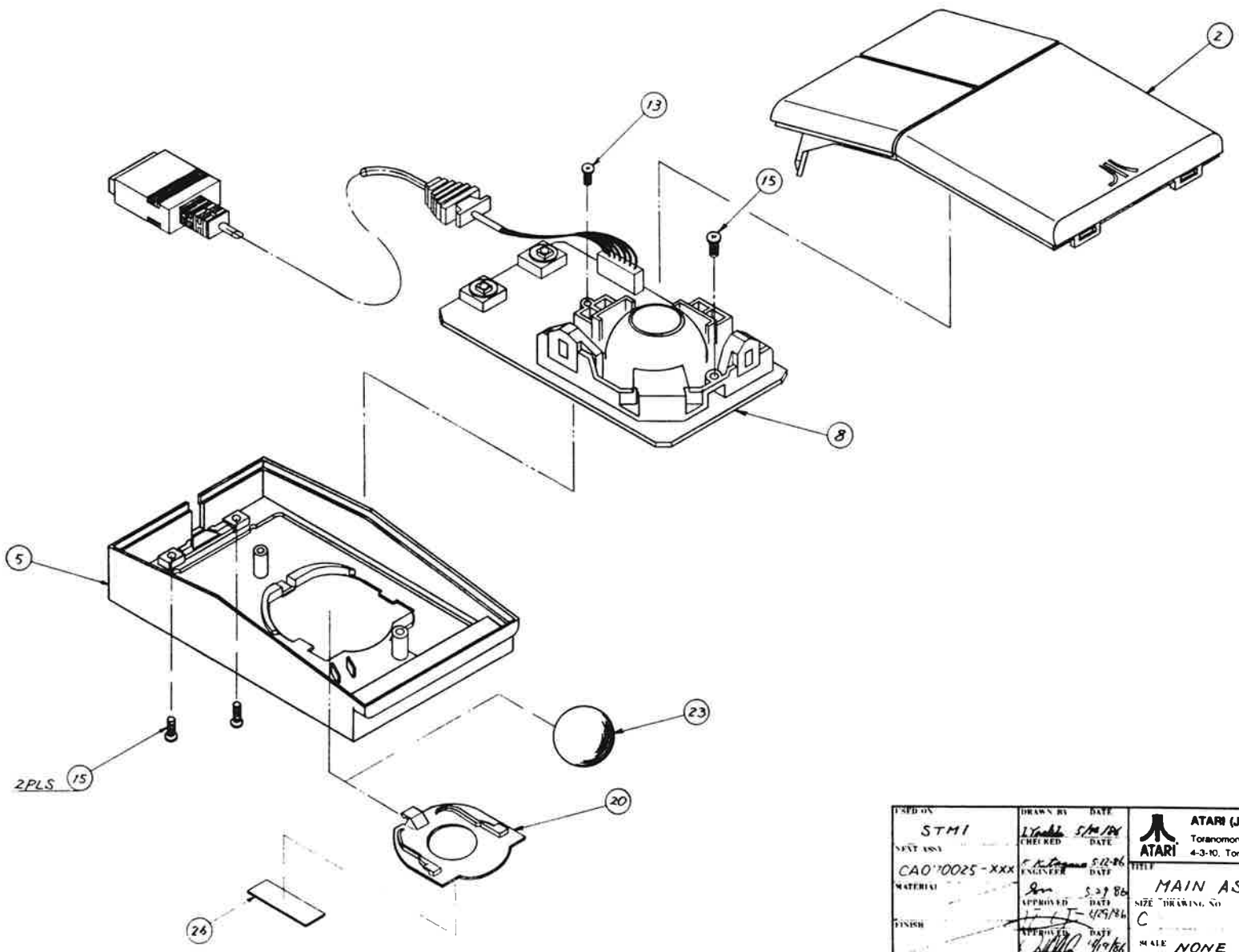
USED ON	DRAWN BY	DATE	ATARI (JAPAN) CORPORATION
MEGA ST2	N.T	16-87	Toranomon Kiyoshi Building
NEXT ASSY	CHECKED	DATE	4-3-10, Toranomon Minato-ku, Tokyo 105
	K.K	9-1-87	
MATERIAL	ENGINEER	DATE	TITLE
		9/10/87	PCB ASSY MEGA
FINISH	APPROVED	DATE	SIZE DRAWING NO / REV
		9/10/87	C / A
	APPROVED	DATE	SCALE NONE SHEET 6 OF 6
	OHASHI	9/10/87	

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON	DRAWN BY	DATE	ATARI (JAPAN) CORPORATION
MEGA ST (KEYBOARD)		11-2-87	Toranomon Kyoshi Building 3F
NEXT ASSY	CHECKED	DATE	4-3-10, Toranomon Minato-ku, Tokyo 105
		1-20-87	TITLE KEYBOARD MAIN ASSY
MATERIAL	ENGINEER	DATE	MEGA
	APPROVED	DATE 1/21/87	SIZE C DRAWING NO REV A
FINISH	APPROVED	DATE 2/6/87	SCALE NONE SHEET 3 OF 3

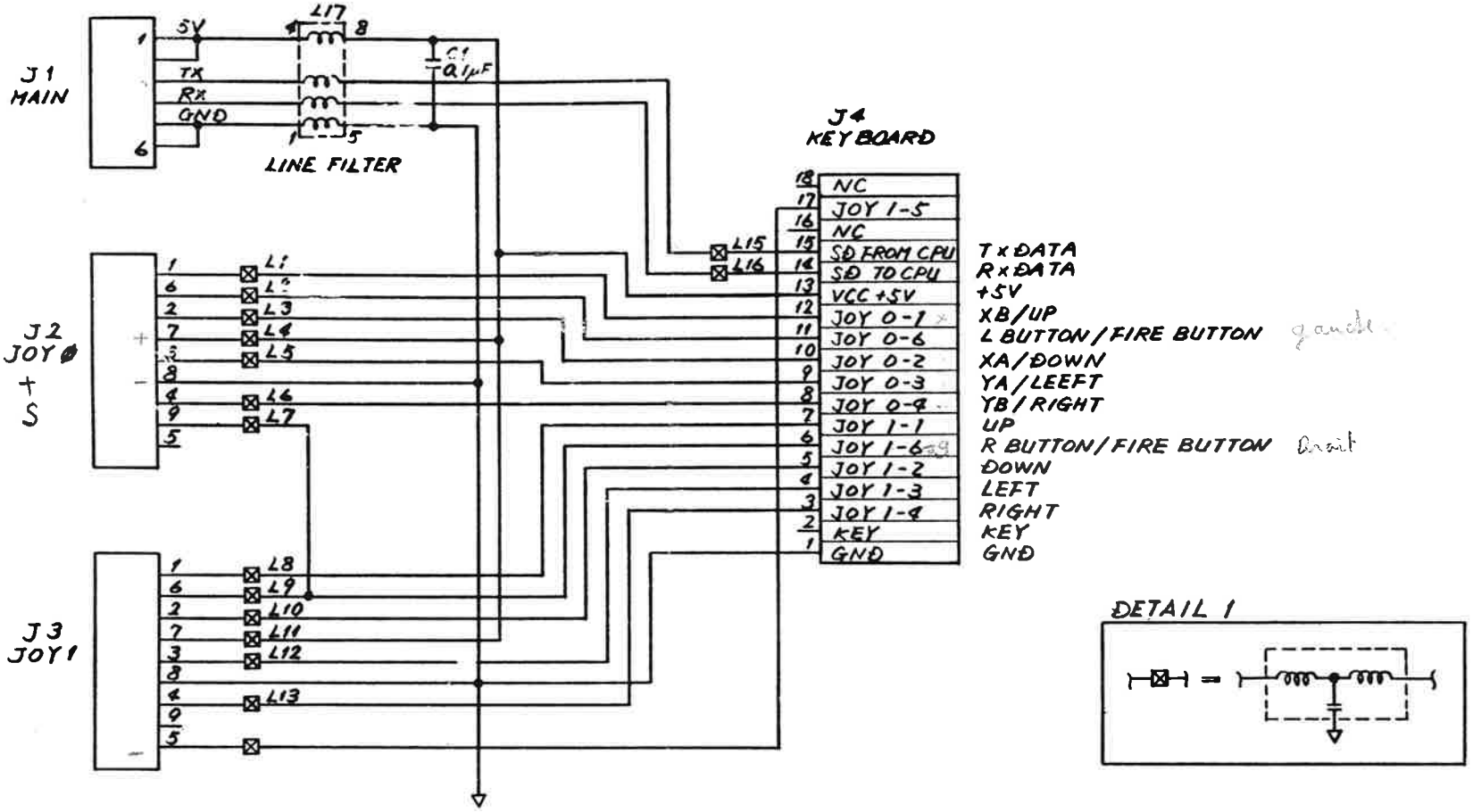
REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON: STM1	DRAWN BY: L Yoshi DATE: 5/30/86	ATARI (JAPAN) CORPORATION
NEXT ASSY: CA0'10025-XXX	CHECKED: DATE	Toranomon Kiyoshi Building 3F
MATERIAL:	ENGINEER: K Kagawa DATE: 5-12-86	4-3-10, Toranomon Minato-ku, Tokyo 105
FINISH:	APPROVED: DATE: 5.29.86	TITLE: MAIN ASSY STM1
	APPROVED: DATE: 4/29/86	SIZE: C DRAWING NO: REV: B
	APPROVED: DATE: 4/29/86	SCALE: NONE SHEET 3 OF 3

SECTION EIGHT
SCHEMATICS AND SILKSCREEN

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	1/8/87	



DETAIL 1

1. NOISE FILTER : SEE DETAIL 1 .

NOTES—UNLESS OTHERWISE SPECIFIED:

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY	USED ON
CA2000X2-XXX	MEGA ST (KEYBOARD)

APPLICATION

	DRAWN BY	DATE
	T. Yoshida	10-26-86
	CHECKED	DATE
	K. Kagawa	10-27-86
	ENGINEER	DATE
	A. Shinogawa	2-16-87
	APPROVED	DATE
	S. OKAZAKI	2/17/87
	APPROVED	DATE
		2/17/87

ATARI

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

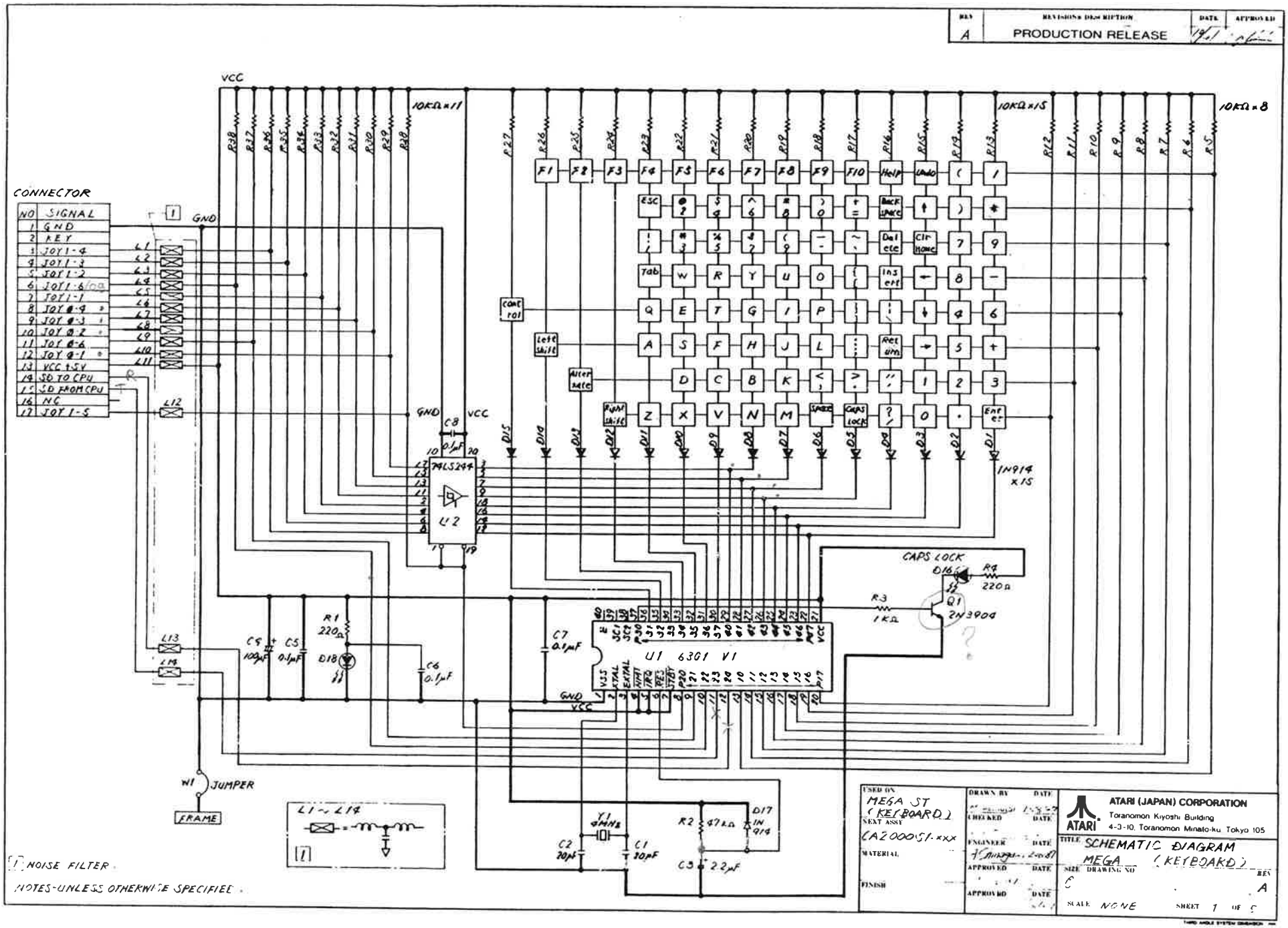
TITLE SCHEMATIC DIAGRAM SUB PCB
MEGA (KEYBOARD)

SIZE	DRAWING NO.	REV
B		A

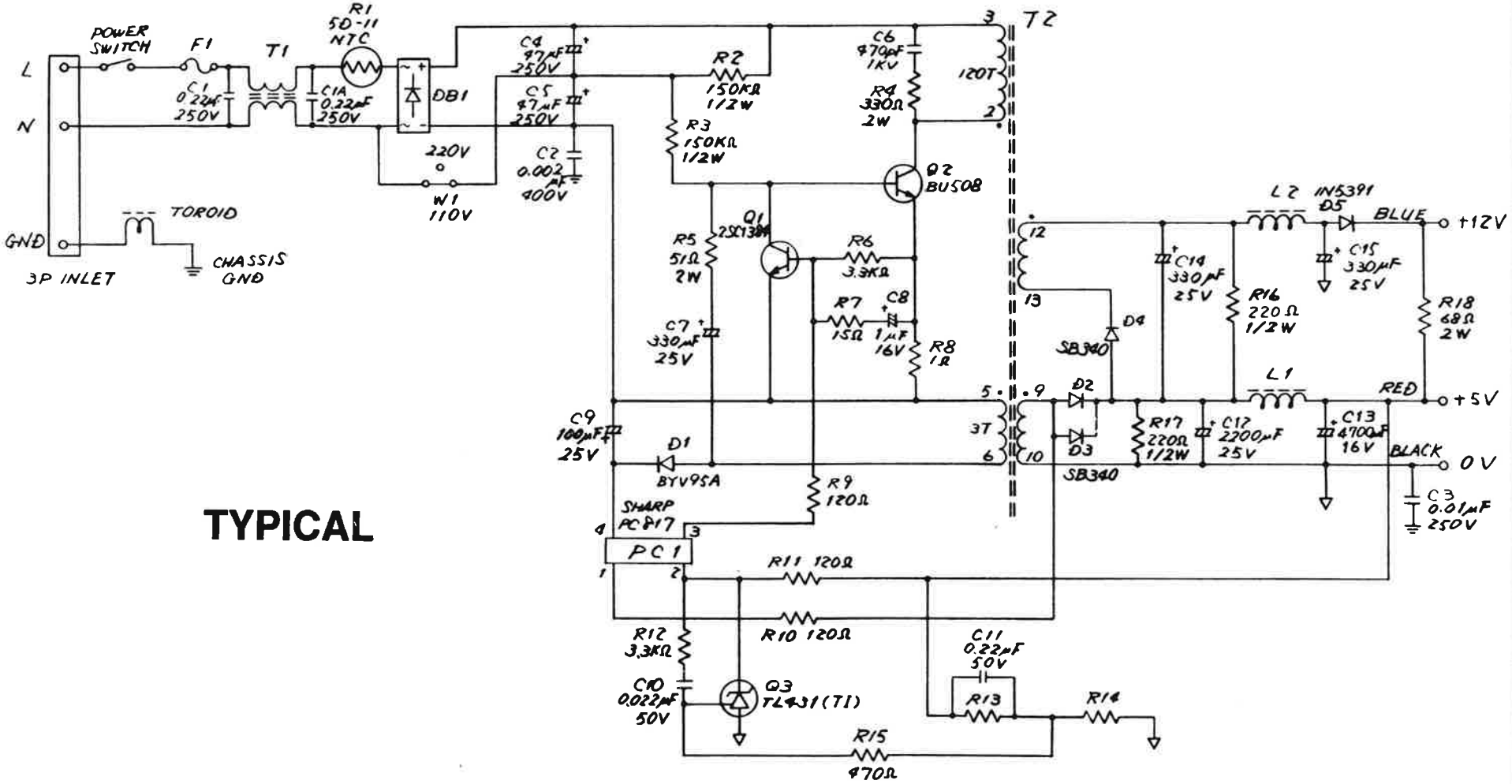
SCALE NONE

SHEET 1 OF 1

THIRD ANGLE SYSTEM. DIMENSION : mm


REV
REVISIONS DESCRIPTION
DATE
APPROVED
A
PRODUCTION RELEASE
CONNECTOR
NO SIGNAL
1 GND
2 KEY
3 JOY1-4
4 JOY1-3
5 JOY1-2
6 JOY1-6/mo
7 JOY1-1
8 JOY0-4
9 JOY0-3
10 JOY0-2
11 JOY0-6
12 JOY0-1
13 VCC +5V
14 SD TO CPU
15 SD FROM CPU
16 NC
17 JOY1-5
VCC
GND
10KΩ×11
10KΩ×15
10KΩ×8
R38 R37 R36 R35 R34 R33 R32 R31 R30 R29 R28
R27 R26 R25 R24 R23 R22 R21 R20 R19 R18 R17 R16 R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 Help Undo (/
ESC ! @ # $ % ^ & *) + Back space
Tab Q W E R T Y U I O P { [Insert ← 7 8 9 −
control A S D F G H J K L : ; Return → 4 5 6 +
Left shift Z X C V B N M < , > . ? / Right shift 1 2 3
Alternate SPACE CAPS LOCK 0 . Enter
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
1N914 ×15
L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14
C8 0.1μF
74LS244
U2
U1 6301 V1
C7 0.1μF
C6 0.1μF
C5 0.1μF
C4 100μF
R1 220Ω
D18
CAPS LOCK
D16
R4 220Ω
R3 1KΩ
Q1 2N3906
W1 JUMPER
FRAME
L1 ~ L14
Y1 4MHz
C2 20pF
C1 30pF
R2 47kΩ
D17 1N914
C3 22μF
[1] NOISE FILTER.
NOTES-UNLESS OTHERWISE SPECIFIED.
USED ON
MEGA ST (KEYBOARD)
NEXT ASSY
CA200051-xxx
MATERIAL
FINISH
DRAWN BY DATE
CHECKED DATE
ENGINEER DATE
APPROVED DATE
APPROVED DATE
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4-3-10, Toranomon Minato-ku Tokyo 105
TITLE SCHEMATIC DIAGRAM
MEGA (KEYBOARD)
SIZE C
DRAWING NO
REV A
SCALE NONE
SHEET 1 OF 5

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	5/20/87	



TYPICAL

TOLERANCES	
UNDER 30	± 0.1
30 THRU 300	± 0.2
OVER 300	± 0.4

USED ON: ASP34-1
NEXT ASSY:
MATERIAL:
FINISH:

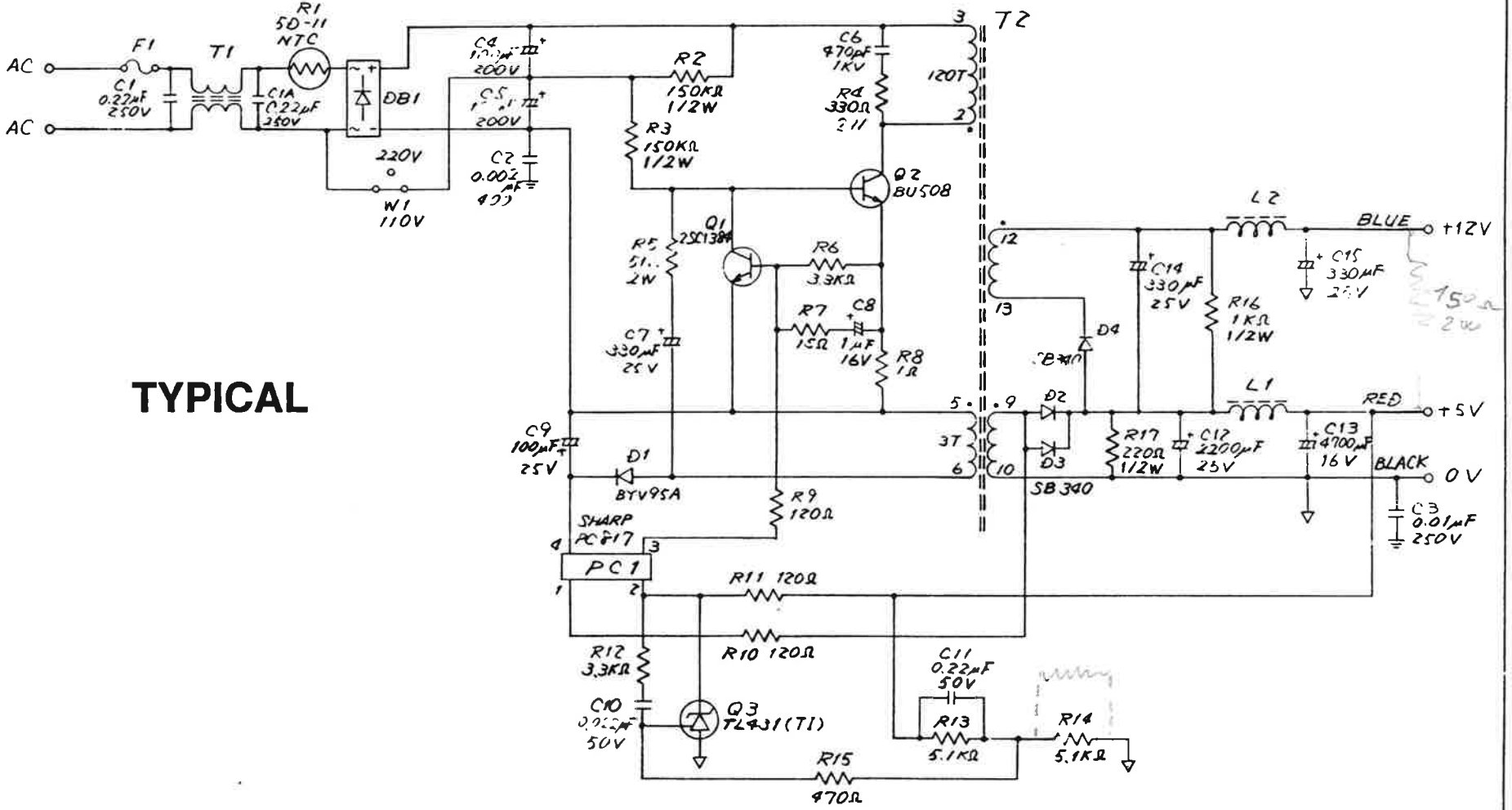
DRAWN BY: I. Yoshida DATE: 9/23/86
CHECKED: K. Kitagawa DATE: 9-18-86
ENGINEER: A. Shimagawa DATE: 10-23-86
APPROVED: DATE:
APPROVED: DATE: 10/23/86

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

TITLE: SCHEMATIC DIAGRAM (ASP34-1)
SIZE: B DRAWING NO.: COMPUTER REV: A
SCALE: NONE SHEET: 1 OF 1

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE		



TYPICAL

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

USED ON: ASP-3

NEXT ASSY

MATERIAL

FINISH

DRAWN BY	I Yoshida	DATE 9/23/86
CHECKED		DATE 9/18/86
ENGINEER	T. Kimagawa	DATE 10/29/86
APPROVED		DATE
APPROVED		DATE

ATARI

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku Tokyo 105

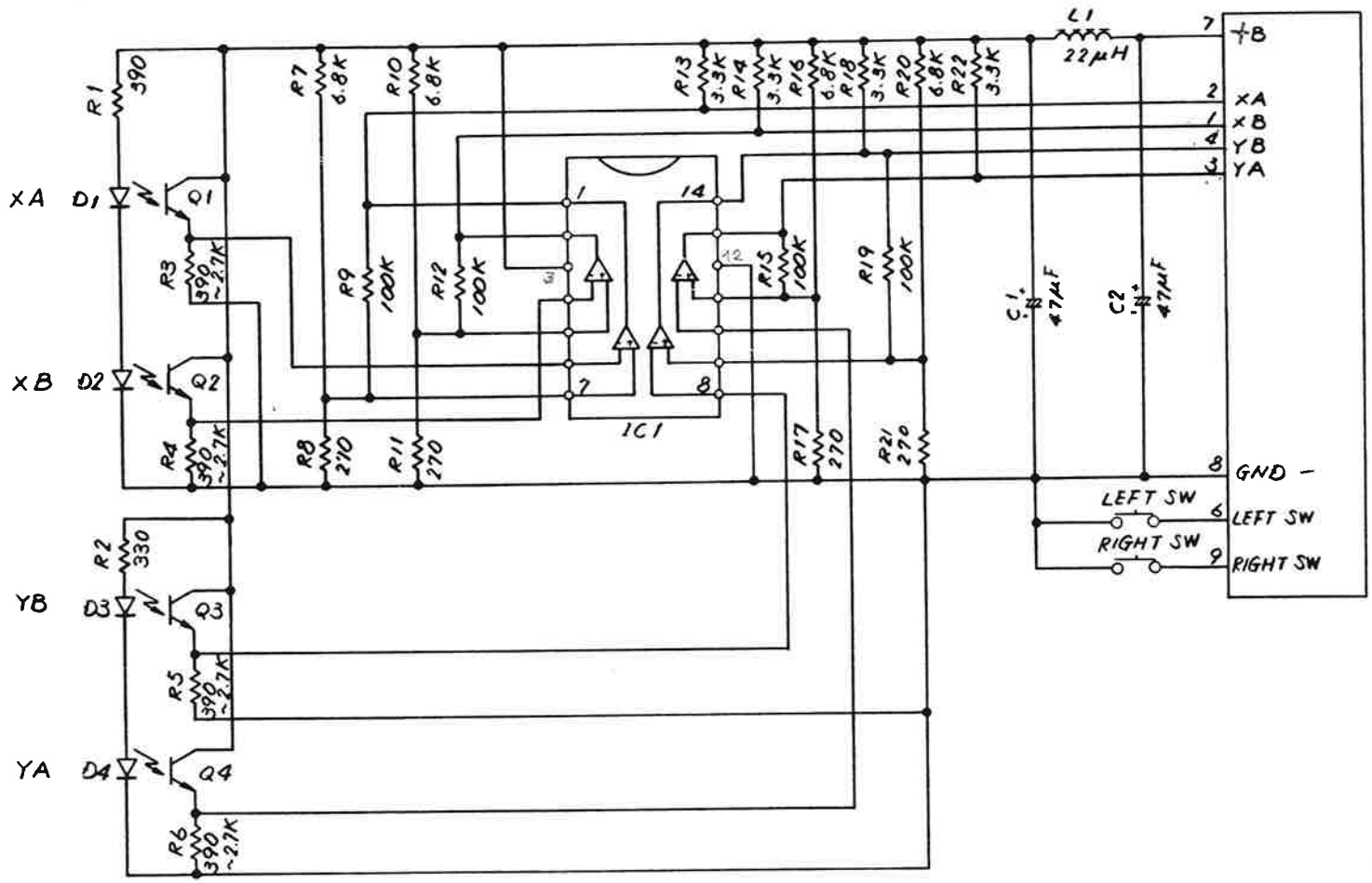
TITLE: SCHEMATIC DIAGRAM (ASP3A-3)

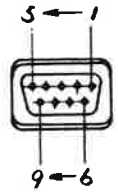
SIZE: B | DRAWING NO: HARD DRIVE | REV: A

SCALE: NONE | SHEET 1 OF 1

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	7/9/87	





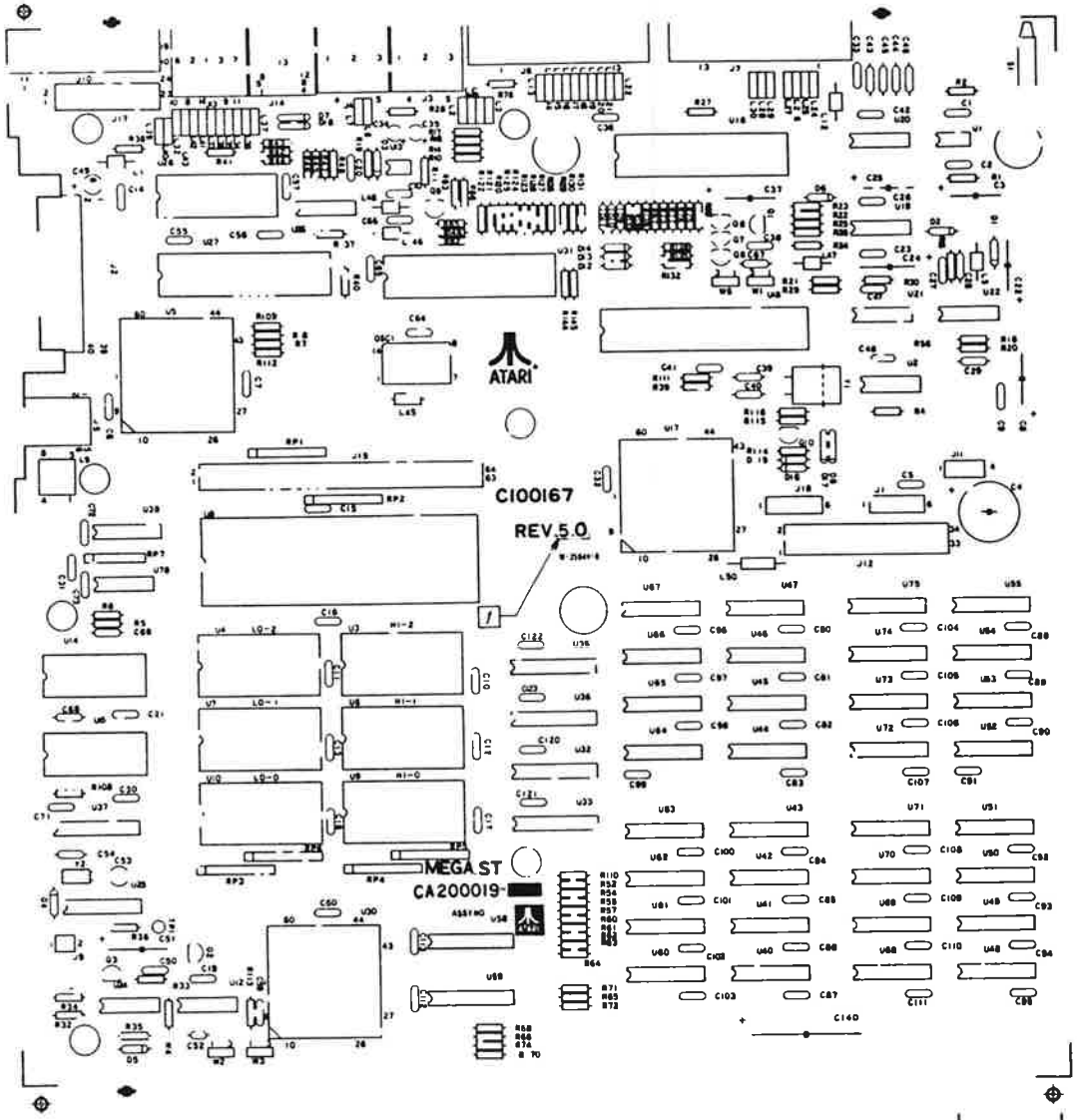
3. IC1 : μPC339G OR TA75339F OR EQUIVALENT
2. Q1 ~ Q4 : PHOTO TRANSISTOR LTR301 OR EQUIVALENT.
1. D1 ~ D4 : LED LTE-301 OR EQUIVALENT.

NOTES - UNLESS OTHERWISE SPECIFIED:

USED ON: STM1	DRAWN BY: H. Kamamata	DATE: 5-28-85	ATARI (JAPAN) CORPORATION Toranomon Kiyoshi Building 3F 4-3-10, Toranomon Minato-ku, Tokyo 105
NEXT ASSY	CHECKED: K. Kitagawa	DATE: 9-17-86	TITLE: SCHEMATIC DIAGRAM (MOUSE)
MATERIAL	ENGINEER: A. Shinagawa	DATE: 10-7-86	SIZE: B — DRAWING NO. — REV: A
FINISH	APPROVED: S. Otaki	DATE: 10/14/86	SCALE: NONE — SHEET 1 OF 1
	APPROVED:	DATE: 10/15/86	

THIRD ANGLE SYSTEM DIMENSION mm

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



SILK PRINT

NOTES—UNLESS OTHERWISE SPECIFIED

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY — DATE 6.15.87

CHECKED — DATE

ENGINEER — DATE

APPROVED — DATE

APPROVED — DATE

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4 3 10, Toranomon Minato ku, Tokyo 105

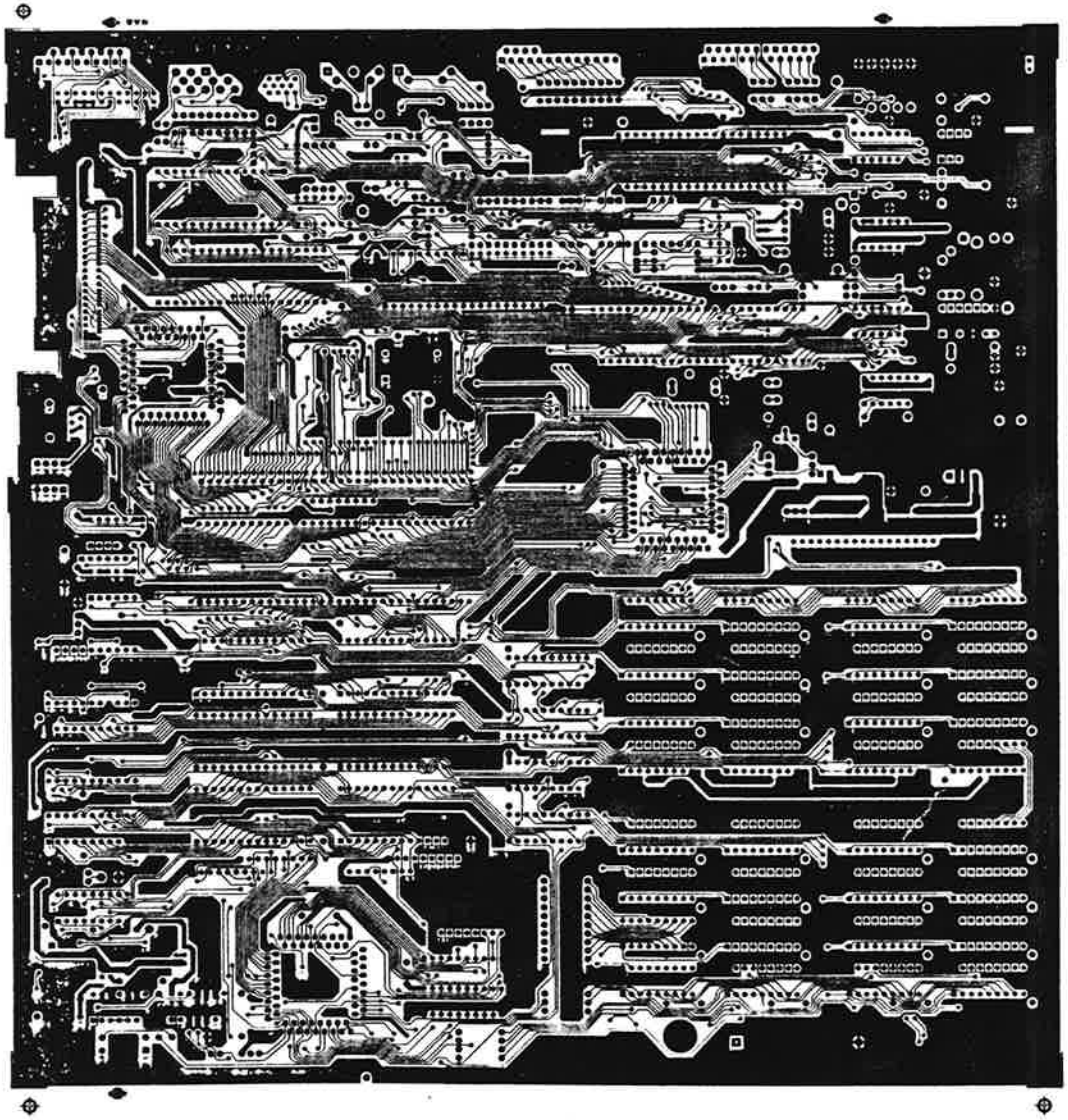
TITLE: PCB MEGA

SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 2 OF 6

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



COMPONENT SIDE

NOTES—UNLESS OTHERWISE SPECIFIED:

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY N. Kawamura DATE 6.15.87

CHECKED DATE

ENGINEER DATE

APPROVED DATE

APPROVED DATE

ATARI

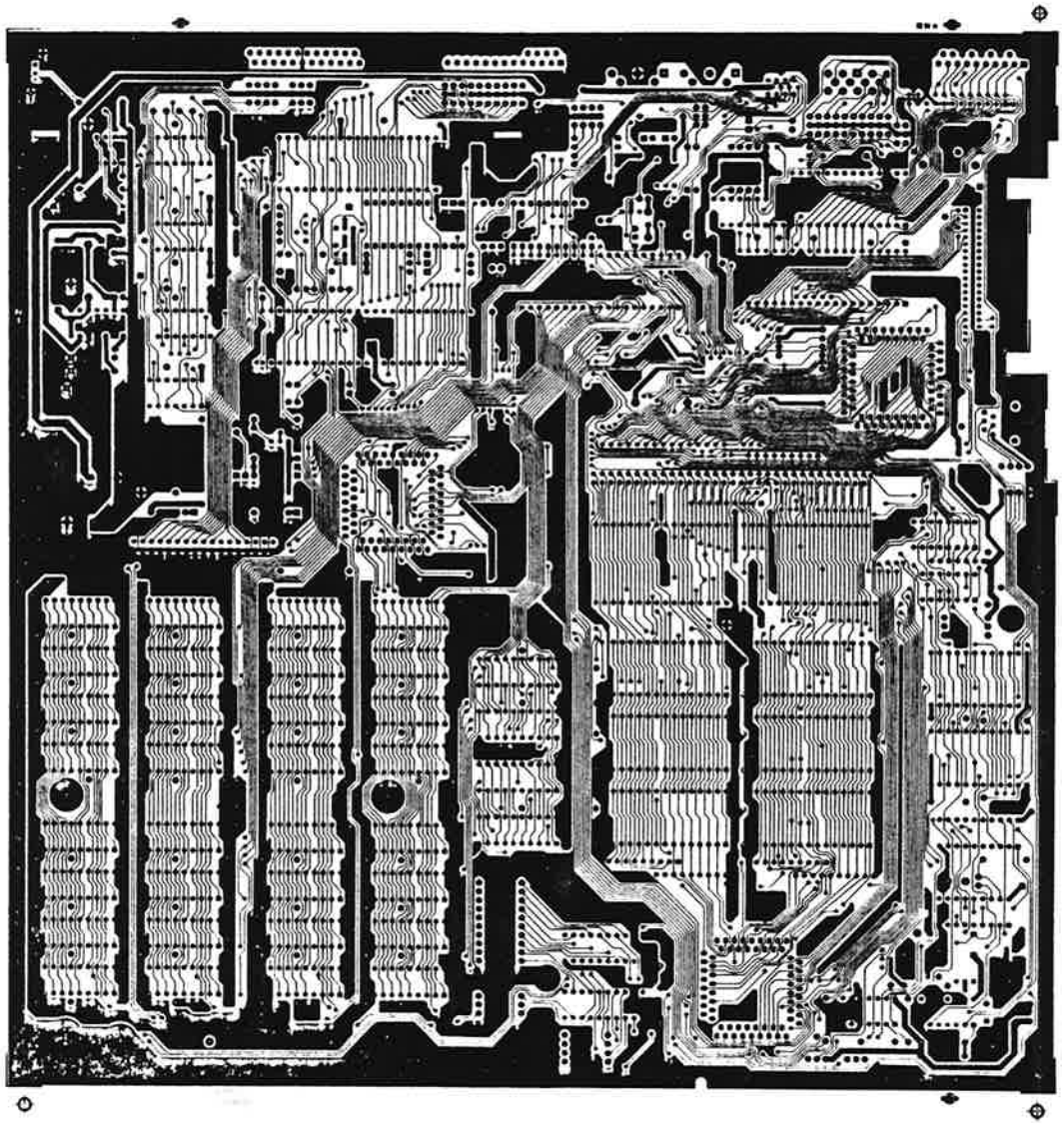
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4 3 10, Toranomon Minato ku Tokyo 105

TITLE PCB MEGA

SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 3 OF 6

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



SOLDER SIDE

NOTES—UNLESS OTHERWISE SPECIFIED

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DRAWN BY Nakamura DATE 6.13.87

CHECKED DATE

ENGINEER DATE

APPROVED DATE

APPROVED DATE

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4 3 10, Toranomon Minato ku Tokyo 105

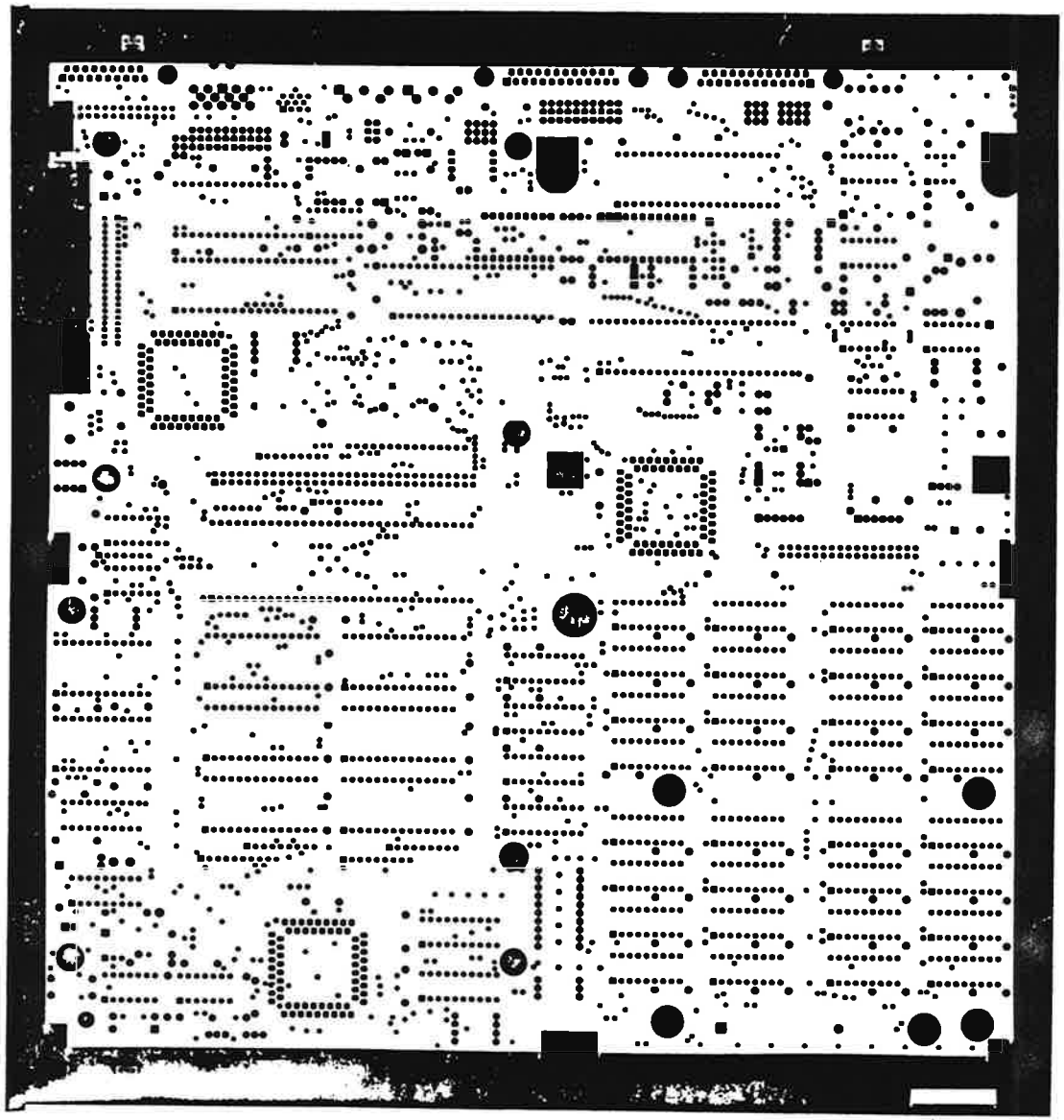
TITLE PCB MEGA

SIZE C | DRAWING NO | REV A

SCALE NONE | SHEET 4 OF 6

THIRD ANGLE SYSTEM DIMENSION

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



SOLDER MASK
COMPONENT SIDE

NOTES – UNLESS OTHERWISE SPECIFIED.

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

NEXT ASSY	USED ON
APPLICATION	

DRAWN BY	DATE 6/15/87
CHECKED	DATE
ENGINEER	DATE
APPROVED	DATE
APPROVED	DATE

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4-3-10, Toranomon Minato-ku, Tokyo 105

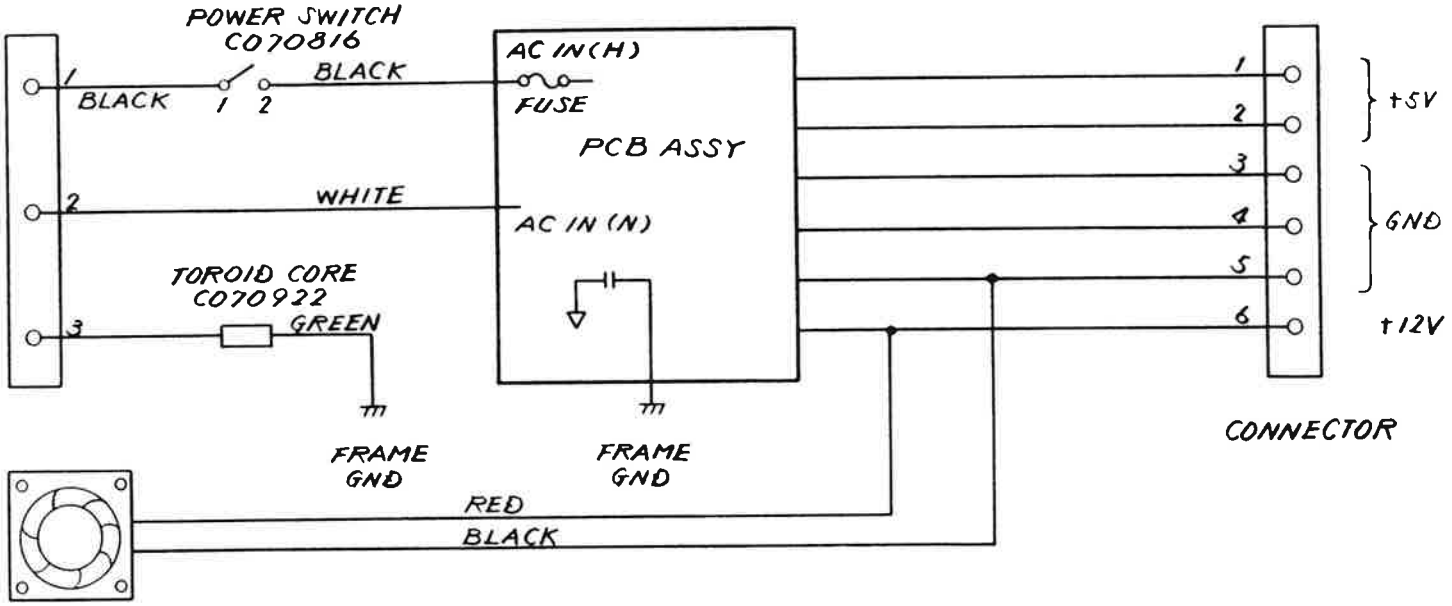
TITLE: PCB MEGA

SIZE C | DRAWING NO | REV A

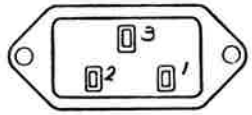
SCALE NONE | SHEET 5 OF 6

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		

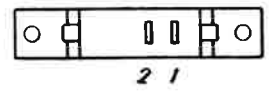
POWER SOCKET
C070815-001



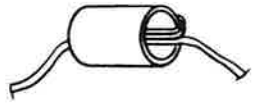
FAN
C100215-011



POWER SOCKET
(REAR VIEW)



POWER SWITCH
(REAR VIEW)



TOROID CORE WIRING
3 TURNS

NOTES—UNLESS OTHERWISE SPECIFIED:

NEXT ASSY	USED ON
	ASP34-1

APPLICATION

TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

MATERIAL

FINISH

DRAWN BY	DATE
H.Kawamata	2-4-87
CHECKED	DATE
ENGINEER	DATE
A.Shinagawa	2-20-87
APPROVED	DATE
N. OKAZAKI	2/20/87
APPROVED	DATE
	2/20/87

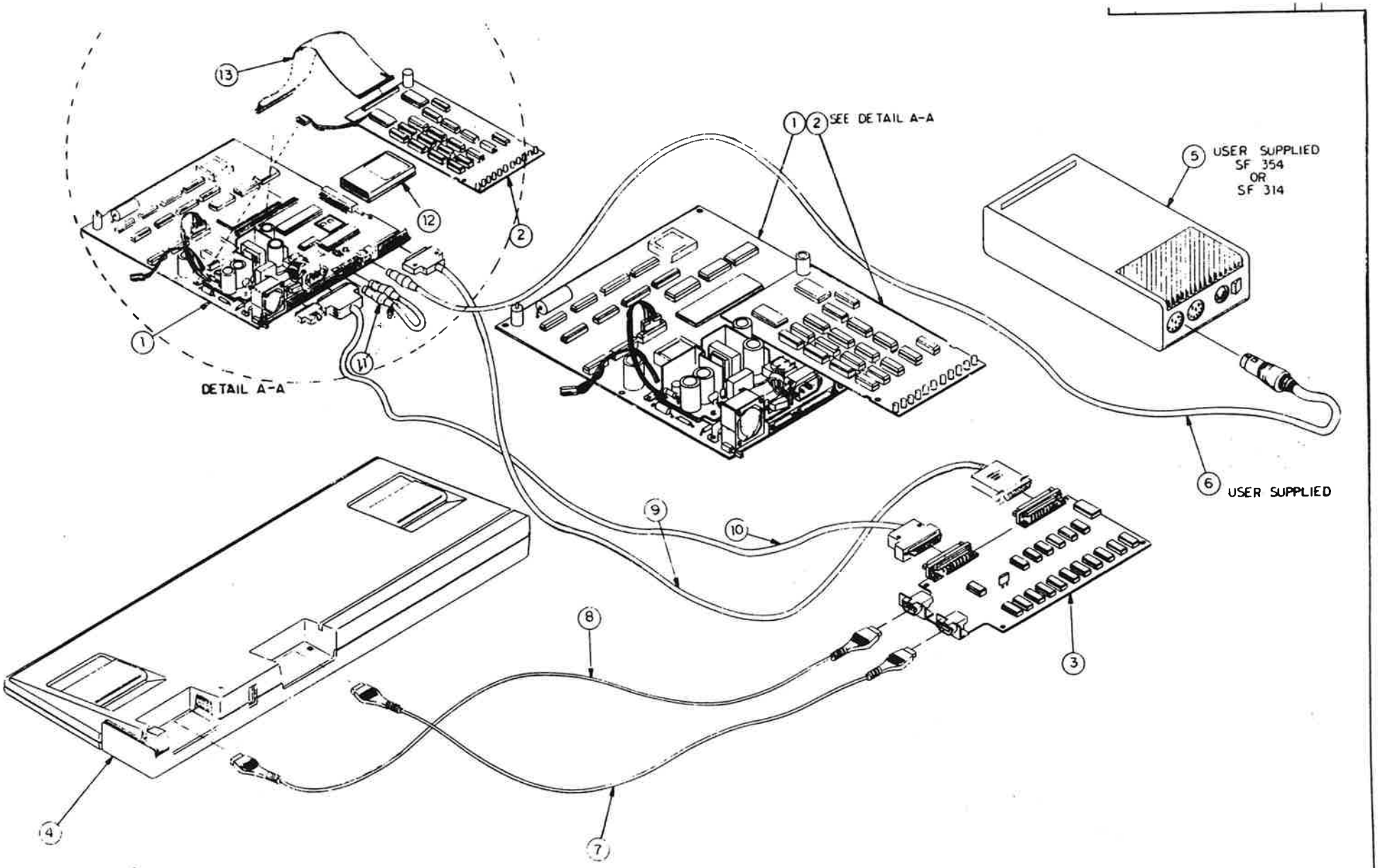
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building
4-3-10, Toranomon Minato-ku, Tokyo 105

TITLE: POWER SUPPLY ASSY
ASP34-1 (117V)

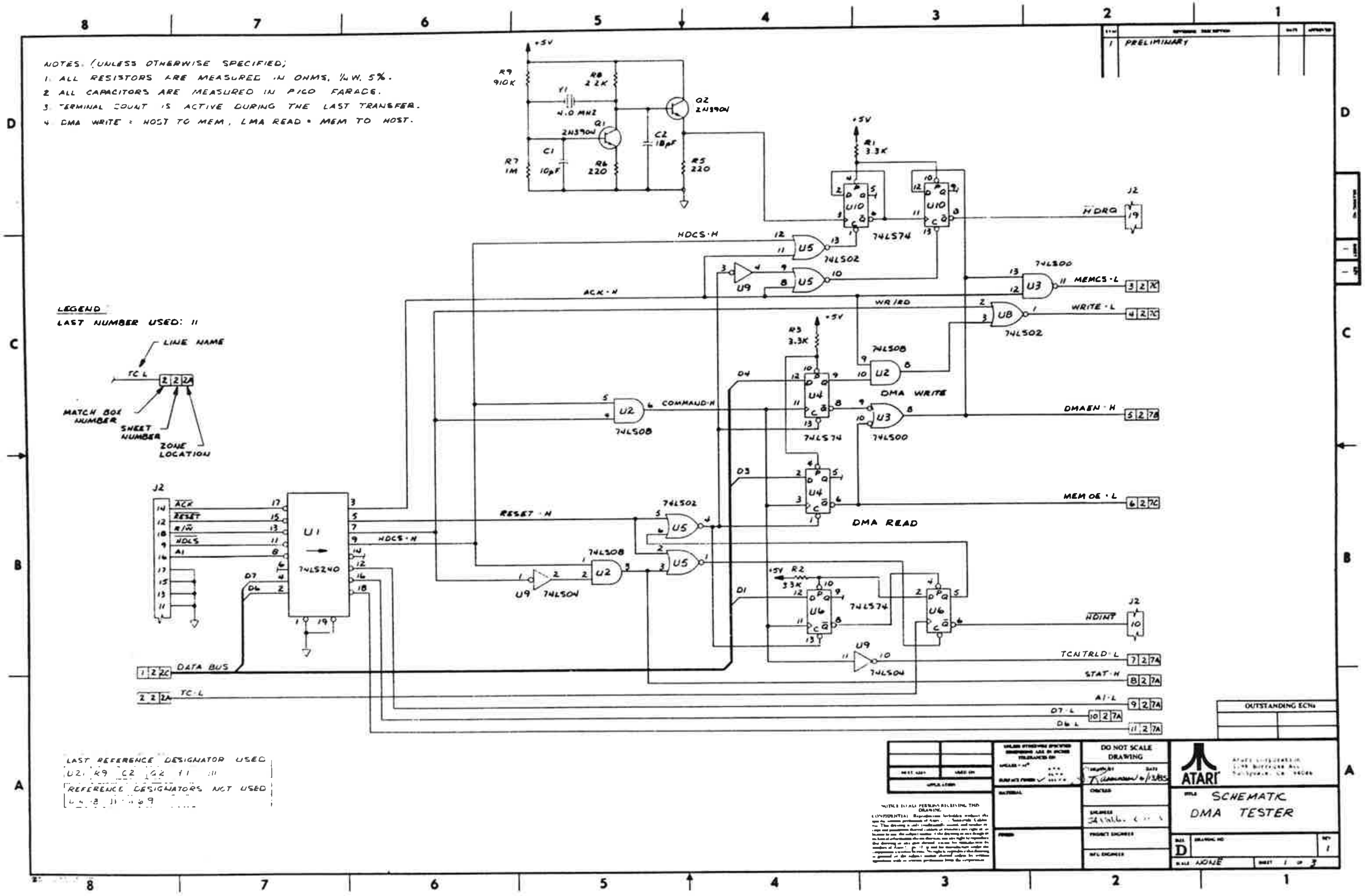
SIZE	DRAWING NO	REV
B		B

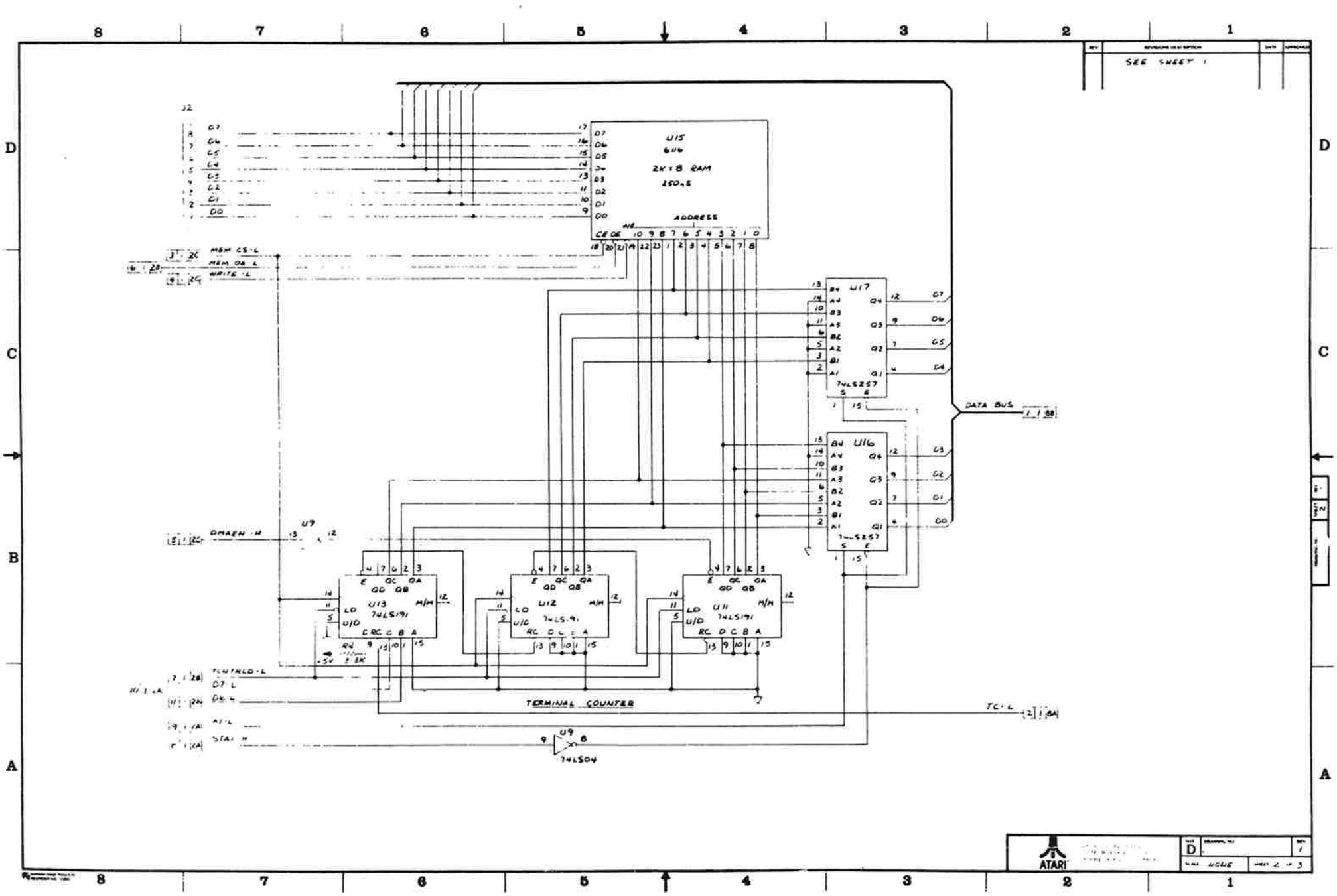
SCALE NONE SHEET 5 OF 5

THIRD ANGLE SYSTEM DIMENSION mm

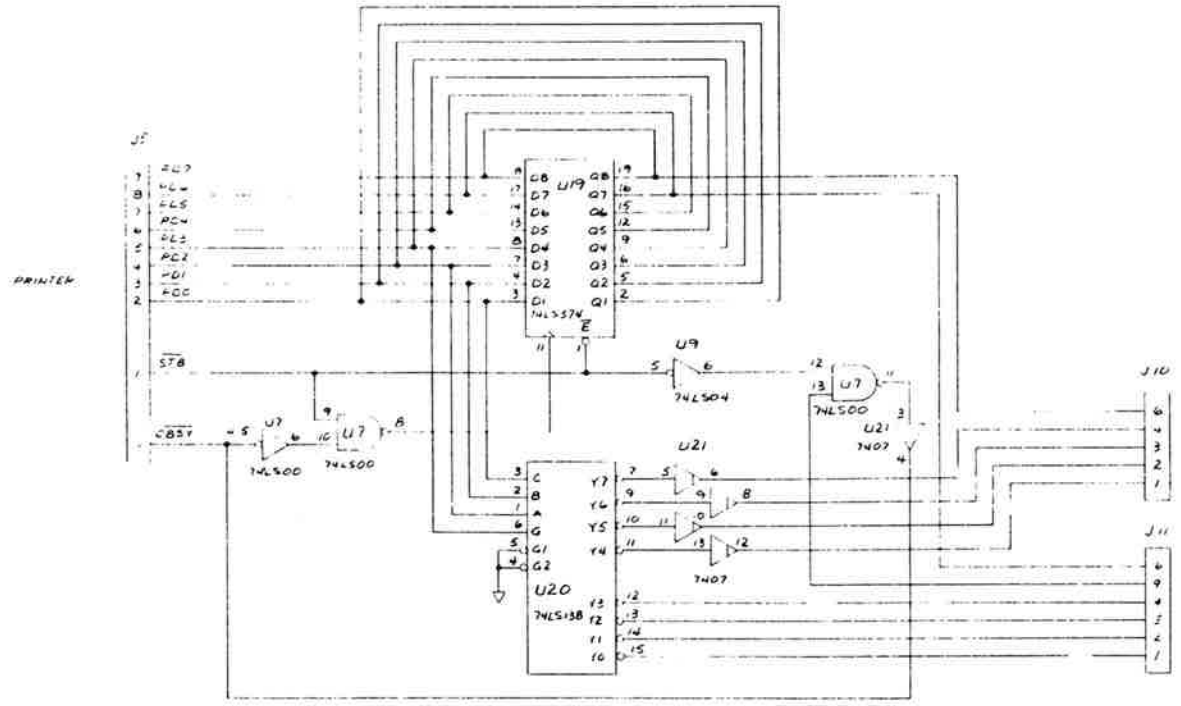


		ATARI (JAPAN) CORPORATION
		ASSY MEGA DIAGNOSTICS
		D A
		SHEET 1 OF 2


NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE MEASURED IN OHMS, 1/4 W, 5%.
2. ALL CAPACITORS ARE MEASURED IN PICO FARADS.
3. TERMINAL COUNT IS ACTIVE DURING THE LAST TRANSFER.
4. DMA WRITE = HOST TO MEM, DMA READ = MEM TO HOST.
LEGEND
LAST NUMBER USED: 11
LINE NAME
MATCH BOX NUMBER
SHEET NUMBER
ZONE LOCATION
PRELIMINARY
HDRQ
MEMCS·L
WRITE·L
DMAEN·H
MEM OE·L
HDINT
TCNTRLD·L
STAT·H
A1·L
D7·L
D6·L
DATA BUS
TC·L
HDCS·H
ACK·H
WR/RD
COMMAND·H
RESET·H
DMA WRITE
DMA READ
74LS74
74LS02
74LS00
74LS08
74LS04
74LS240
OUTSTANDING ECNs
DO NOT SCALE DRAWING
ATARI
SCHEMATIC
DMA TESTER
D
NONE


SEE SHEET 1
U15
6116
2K x 8 RAM
250nS
ADDRESS
U17
U16
74LS257
DATA BUS
MEM CS L
MEM OE L
WRITE L
DMAEN H
U13
U12
U11
74LS191
TERMINAL COUNTER
TC L
U9
74LS04
ATARI

SEE SHEET 1



JOYSTICK AND PRINTER
TEST FIXTURE

DO NOT SCALE DRAWING	ATARI	SCHEMATIC DMA TESTER	
		SIZE D	REV 1
		NONE	SHEET 5 OF 5

SECTION NINE
GLOSSARY OF PART NAMES AND TERMS

BITBLiT--Atari graphic chip which is actually a DMA device. It is used to transfer block of memory from a source to destination with the patterns and a combination of any logical operations between source and destination which was set up prior to the transfer.

BUS ERROR--Glue has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.

CPU--the 68000 microprocessor.

DMA--direct memory access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, takes place independent of the CPU, so the CPU can be processing while DMA is taking place. Glue arbitrates the bus between the CPU and DMA.

DMA CONTROLLER--Atari proprietary chip which controls the DMA process. All disk I/O goes through this device.

EXCEPTION--a state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also Section Two, System Errors, or a 68000 reference for more detail.

GLUE--Atari proprietary chip which ties together all system timing and control signals.

HALT--state in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bi-directional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert HALT.

HSYNC--timing signal for the video display. Determines when the horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) also is encoded onto IPL1,2 as an interrupt to the CPU.

INTERRUPT--a request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities: the highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and Glue.

MEMORY CONTROLLER--Atari proprietary chip which handles all RAM accesses. See Theory of Operation, Main System and Video Subsystem for details.

MIDI--Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the 1040ST, consists of a 6850 communications chip, driver and receiver chips (74LS04, 74LS05, and PC-900 photocoupler), and an MFP interrupt channel.

MFP--Multi-function Peripheral, also 68901. Interrupt control, timers, and USART for RS232 communication. See Theory of Operation, Main System.

MODULATOR--device which combines video signals R,G,B, VSYNC, and HSYNC into a composite signal for monitors requiring this type input, and also modulates this signal, combined with audio, onto an RF carrier for output to a television.

PHASE LOCKED LOOP--circuit which locks the horizontal sync signal onto the color burst reference frequency for accurate color on the T.V. Without this circuit, colors on the T.V. become unstable, flickering or shifting about on the screen. The PPL may be on a daughter board located in front of the video shield or hand wired onto the main board within the video shield, or (possibly) in later versions, integrated into the printed circuit board.

PSG--Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.

RS232C--Electical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the ST computers, consists of the MFP, PSG, 1488, and 1489 chips.

1772--Western Digital Floppy Disk Controller.

6850--also ACIA (Asynchronous Communication Interface Adapter). Interfaces between 8 bit parallel bus and serial communication bus. In the ST, there are two 6850s, one for keyboard communication, and one for MIDI communication.

68901--see MFP.

SUPERVISOR MODE--state of the CPU in which it is allowed to access all hardware and RAM locations, and perform some priviliged instructions. Determined by the state of a bit in the Status Register. The operating system operates in supervisor mode, and switches to user mode before passing control to an application (although the application can enter supervisor mode if it wishes).

USER MODE--state of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.

VSYNC--signal used for vertical synchronization of CRT display device. Occurs at 70 Hz (monochrome), or 50 or 60 Hz color.

YM2149--see PSG.