WESTERN DIGITAL
## CORPORATION

WD177X-00 Floppy Disk Formatter/Controller

FEATURES

- 28 PIN DIP
- SINGLE 5V SUPPLY
- BUILT-IN DIGITAL DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- SINGLE (FM) AND DOUBLE (MFM) DENSITY
- MOTOR CONTROL (WD1770 AND WD1772)
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- TTL COMPATIBLE
- 8-BIT BI-DIRECTIONAL DATA BUS
- TWO VERSIONS AVAILABLE
  WD1770/WD1773 = STANDARD 179X STEP RATES
  WD1772 = FASTER STEP RATES
- THE WD1773 HAS 100% COMPATIBLE SOFTWARE WITH THE WD1793
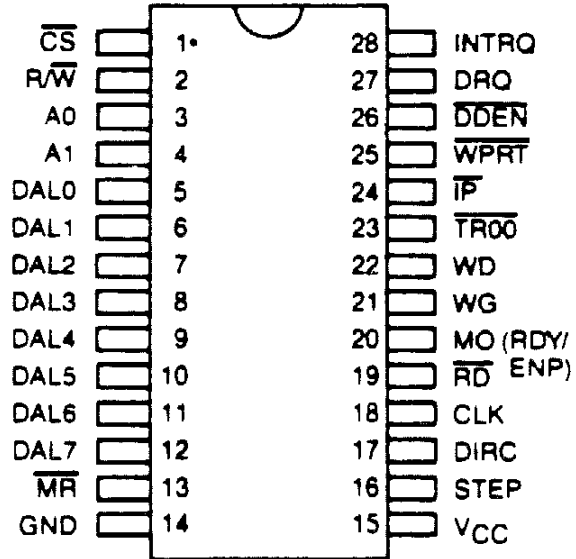
GENERAL DESCRIPTION

The WD177X-00 is a MOS/LSI device which performs the functions of a Floppy Disk Formatter/Controller. It is similar to its predecessor, the FD179X, but also contains a digital data separator and write precompensation circuitry. The drive side of the interface needs no additional logic except for buffers/receivers. It is designed for single (FM) or double (MFM) density operation.

The WD177X-00 is implemented in NMOS silicon gate technology and is available in a 28-pin dual-in-line as well as in quad pack.

Three versions of the WD177X-00 are available. The WD1770, WD1772 and the WD1773.

With the exception of the enable precomp/ready line, the WD1773 is identical to the WD1770 controller. It is fully software compatible with the WD1793. The WD1770-00 and WD1773-00 are compatible with the FD179X stepping rates, while the WD1772-00 offers stepping rates of 2, 3, 6, and 12 msec.

The WD177X-00 devices all contain a built-in digital data separator which virtually eliminates all external components and adjustments associated with data

$\overline{CS}$	1•	28	INTRQ
R/$\overline{W}$	2	27	DRQ
A0	3	26	$\overline{DDEN}$
A1	4	25	$\overline{WPRT}$
DAL0	5	24	$\overline{IP}$
DAL1	6	23	$\overline{TR00}$
DAL2	7	22	WD
DAL3	8	21	WG
DAL4	9	20	MO (RDY/
DAL5	10	19	$\overline{RD}$ ENP)
DAL6	11	18	CLK
DAL7	12	17	DIRC
$\overline{MR}$	13	16	STEP
GND	14	15	V_{CC}

DIP PIN DESIGNATION

recovery in previous designs. A single read line (RD, Pin 19) is the only input required to recover serial FM or MFM data from the disk drive. The device is designed for control of floppy disk drives with data rates of 125 KBits/Sec (single density) and 250 KBits/Sec (double density). In addition, write precompensation of 125 nsec from nominal is enabled at any point through simple software commands. Another programmable feature on the WD1770/WD1772 is Motor On, which enables the spindle motor automatically prior to operating a selected drive.

The processor interface consists of an 8-bit bi-directional bus for transfer of status, data, and commands. All Host communication with the drive occurs through these lines. They are capable of driving one standard TTL load or three LS loads.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{CS}$	CHIP SELECT	I	A logic low on this input selects the chip and enables Host communication with the device.
2	R/$\overline{W}$	READ/WRITE	I	A logic high on this input controls the placement of data on the D0-D7 lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	A0,A1	ADDRESS 0,1	I	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Commad Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DAL0-DAL7	DATA ACCESS LINES 0 THROUGH 7	I/O	Eight-bit bi-directional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/W. Each line will drive one TTL load.
13	$\overline{MR}$	MASTER RESET	I	A logic low pulse on this line resets the device and initializes the Status Register (internal pull-up).
14	GND	GROUND		Ground.
15	V_{CC}	POWER SUPPLY	I	+5V±5% power supply input.
16	STEP	STEP	O	The Step output contains a pulse for each step of the drive's R/W head. The WD1770-00 and WD1772-00 offer different step rates.
17	DIRC	DIRECTION	O	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLK	CLOCK	I	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHz +0.1%.
19	$\overline{RD}$	READ DATA	I	This active low input is the raw data line containing both clock and data pulses from the drive.
20	RDY/ENP	READY/ENABLE PRECOMP (WD1773)	I	Serves as a READY input from the drive during READ/STEP operations and as a Write Precomp enable during Write operations. The state of READY is latched upon WG true, and this dual input is used for precompensation enable.
20	MO	MOTOR ON (WD1770 or WD-1772)	O	Active high output used to enable the spindle motor prior to read, write or stepping operations. (WD1770, WD1772 only)
21	WG	WRITE GATE	O	This output is made valid prior to writing on the diskette.
22	WD	WRITE DATA	O	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This active low input informs the WD1770-00 that the drive's R/W heads are positioned over Track zero.
24	$\overline{IP}$	$\overline{INDEX\ PULSE}$	I	This active low input informs the WD1770-00 when the physical index hole has been encountered on the diskette.
25	$\overline{WPRT}$	$\overline{WRITE\ PROTECT}$	I	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up).

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
26	DDEN	DOUBLE DENSITY ENABLE	I	This input pin selects either single (FM) or double (MFM) density. When DDEN = 0, double density is selected (internal pull-up).
27	DRQ	DATA REQUEST	O	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTRQ	INTERRUPT REQUEST	O	This active high output is set at the completion of any command, is reset by a read of the Status Register.
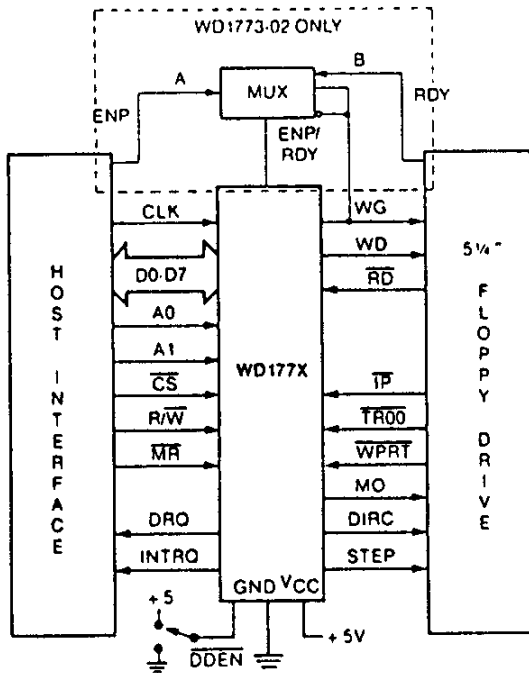
WD177X-02 SYSTEM BLOCK DIAGRAM

ARCHITECTURE

The primary sections of the Floppy Disk Formatter are the Parallel Processor Interface and the Floppy Disk Interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input (RD) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register – This 8-bit register is used as a holding register during Disk Read and Write operations. In disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek Command, the Data Register holds the address of the desired Track posi-

tion. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register is not loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register is not loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register is not loaded when the device is busy unless the new command is a force interrupt. The Command Register is loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register is read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:
$$G(x) = x^{16} + x^{12} + x^5 + 1.$$
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC Register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.
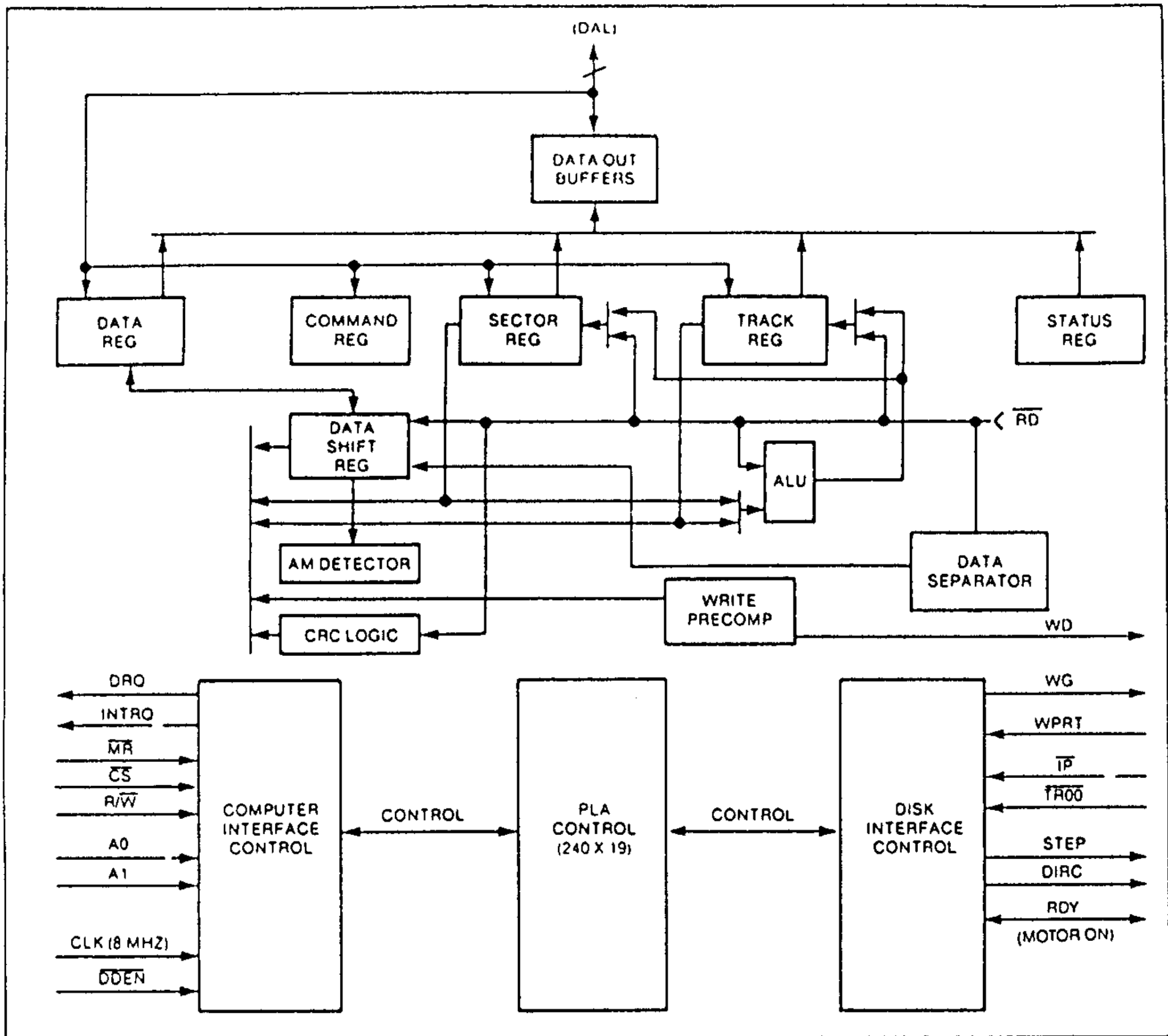
FIGURE 1. WD177X-00 BLOCK DIAGRAM

Timing and Control – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The WD177X-00 has two different modes of operation according to the state of DDEN.

When $\overline{\text{DDEN}}$ = 0, double density (MFM) is enabled. When $\overline{\text{DDEN}}$ = 1, single density is enabled.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Data Separator – A digital data separator consisting of a ring shift register and data window detection logic provides read data and a recovery clock to the AM detector.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD177X-00. The DAL are three state buffers that are enabled as output drivers when $\overline{\text{CS}}$ and R/W = 1 are active or act as input receivers when $\overline{\text{CS}}$ and R/W = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the Host processor, the device address is decoded and $\overline{\text{CS}}$ is made low. The address bits A1 and A0, combined with the signal R/W during a Read operation or Write operation are interpreted as selecting the following registers:

A1 - A0		READ (R/W̄ = 1)	WRITE (R/W̄ = 0)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

After any register is written to, the same register cannot be read from until 16 μsec in MFM or 32 μsec in FM have elapsed.

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD177X-00 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request bit is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operations continue until the end of sector is reached.

On Disk Write operations the Data Request bit is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt Command condition is met.

The WD177X-00 has two modes of operation according to the state DDEN. When DDEN = 1, single density is selected. In either case, the CLK input is at 8 MHz.

GENERAL DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, DDEN is placed to logical 1. For MFM formats, DDEN is placed to a logical 0. Sector lengths are determined at format time by the fourth byte in the ID field.

SECTOR LENGTH TABLE	
SECTOR LENGTH FIELD (HEX)	NUMBER OF BYTES IN SECTOR (DECIMAL)
00	128
01	256
02	512
03	1024

The number of sectors per track for the WD177X-00 are from 1 to 240. The number of tracks for the WD177X-00 are 0 to 240.

GENERAL DISK WRITE OPERATION

When writing on the diskette the WG output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte is loaded into the Data Register in response to a Data Request from the device before the WG is activated.

Writing is inhibited when the WPRT input is asserted, in which case any Write Command is immediately terminated, an interrupt is generated and the Write Protect Status bit is set.

For Write operations, the WD177X-00 provides WG to enable a Write condition, and WD which consists of a series of active high pulses. These pulses contain both Clock and Data information in FM and MFM. WD provides the unique missing clock patterns for recording Address Marks.

The WD1773-00 enables write precompensation when RDY/ENP is asserted. When WG is asserted the READY status has been latched. WG is then used to demultiplex drive Ready Status from Host supplied enable for write precompensation at desired tracks.

On the WD1770-02 or WD1772-00, the Precomp Enable bit in Write Commands allows automatic Write precompensation to take place. The outgoing Write Data stream is delayed or advanced from nominal by 125 nsec according to the following table:

PATTERN				MFM	FM
X	1	1	0	Early	N/A
X	0	1	1	Late	N/A
0	0	0	1	Early	N/A
1	0	0	0	Late	N/A

— Next Bit to be sent
— Current Bit sending
— Previous Bits sent
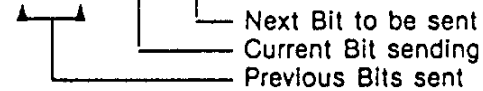
Precompensation is typically enabled on the innermost tracks where bit shifts usually occur and bit density is at its maximum. READY is true for read/write operations (all Type II and III Command executions).

COMMAND DESCRIPTION

The WD177X-00 accepts 11 commands. Command words are only loaded in the Command Register when the Busy Status bit is off (Status bit 0). The one exception is the Force Interrupt Command. Whenever a command is being executed, the Busy Status bit is set. When a command is completed, an interrupt is generated and the Busy Status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. Commands are divided into four types and are summarized in the following pages.

COMMAND SUMMARY

TYPE COMMAND	7	6	5	4	BITS 3	2	1	0
I Restore	0	0	0	0	h	V	r_1	r_0
I Seek	0	0	0	1	h	V	r_1	r_0
I Step	0	0	1	u	h	V	r_1	r_0
I Step-in	0	1	0	u	h	V	r_1	r_0
I Step-out	0	1	1	u	h	V	r	r_0
II Read Sector	1	0	0	m	h/s	E	0/C	0
II Write Sector	1	0	1	m	h/s	E	P/C	a_0
III Read Address	1	1	0	0	h/o	E	0	0
III Read Track	1	1	1	0	h/o	E	0	0
III Write Track	1	1	1	1	h/o	E	P/O	0
IV Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

FLAG SUMMARY

TYPE I COMMANDS

h = Motor On Flag (Bit 3) (1770/2).

h = 0, Enable Spin-up Sequence
h = 1, Disable Spin-up Sequence

V = Verify Flag (Bit 2) (1770/2/3)

V = 0, No Verify
V = 1, Verify on Destination Track

r_1, r_0 = Stepping Rate (Bits 1,0)

		WD1770-00 WD1773-00	WD1772-00
r_1	r_0		
0	0	6 ms	6 ms
0	1	12 ms	12 ms
1	0	20 ms	2 ms
1	1	30 ms	3 ms

u = Update Flag (Bit 4) (1770/2/3)

u = 0, No Update
u = 1, Update Track Register

TYPE II & III COMMANDS

m = Multiple Sector Flag (Bit 4) (1770/2/3)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor on Flag (Bit 3) (1770/2)

H = 0, Enable Spin-up Sequence
H = 1, Disable Spin-up Sequence

S = Side Compare Flag (Bit 3) (1773 only)

S = 0, Compare for side 0
S = 1, Compare ;for side 1
For all Type III commands bit 3 must be 0.

a_0 = Data Address Mark (Bit 0) (1770/2/3)

a_0 = 0, Write Normal Data Mark
a_0 = 1, Write Deleted Data Mark

TYPE II & III COMMANDS (Continued)

E = 30ms Settling Delay (Bit 2) (1770/2/3)

E = 0, No Delay
E = 1, Add 30ms Delay (1772 Add 15ms Delay

C = Side Compare Flag (Bit 1) (1773 only)

C = 0, Disable Side Compare
C = 1, Enable Side Compare
For all Type III commands bit 1 must be 0.

P = Write Precompensation (Bit 1) (1770/2/3)

P = 0, Enable Write Precomp
P = 1, Disable Write Precomp

TYPE IV COMMANDS

I_3-I_0 Interrupt Condition (Bits 3-0)

I_0 = Not Used (WD1770-00, WD1772-00)
    Not Ready to Ready Transition (WD1773-00)
I_1 = Not Used (WD1770-00, WD1772-00)
    Ready to Not Ready Transition (WD1773-00)
I_2 = Interrupt on Index Pulse
I_3 = Immediate Interrupt
I_3-I_0 = Terminate without interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-in, and Step-Out Commands. Each of the Type I Commands contains a rate field (r_0,r_1), which determines the stepping motor rate.

A 4 μsec (MFM) or 8 μsec (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip steps the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 μsec before the first stepping pulse is generated.

After the last directional step an additional *30 msec of head settling time takes place if the Verify flag is set in Type I Commands. There is also a *30 msec head settling time if the E flag is set in any Type II or III Command.

When a Seek, Step or Restore Command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the *30 msec settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field CRC is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not

a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation.

The WD177X-00 finds an ID Field with correct track number and correct CRC within 5 revolutions of the media, or the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

On the WD1770-00 and WD1772-00 only, all commands, except the Force Interrupt Command, are pro-grammed via the h Flag to delay for spindle motor start up time. If the h Flag is not set and the MO signal is low when a command is received, the WD1770/2-00 forces MO to a logic 1 and waits 6 revolutions before executing the command. At 300 RPM, this guarantees a one-second spindle start up time. If after finishing the command, the device remains idle for 9 revolutions, the MO signal goes back to a logic 0. If a command is issued while MO
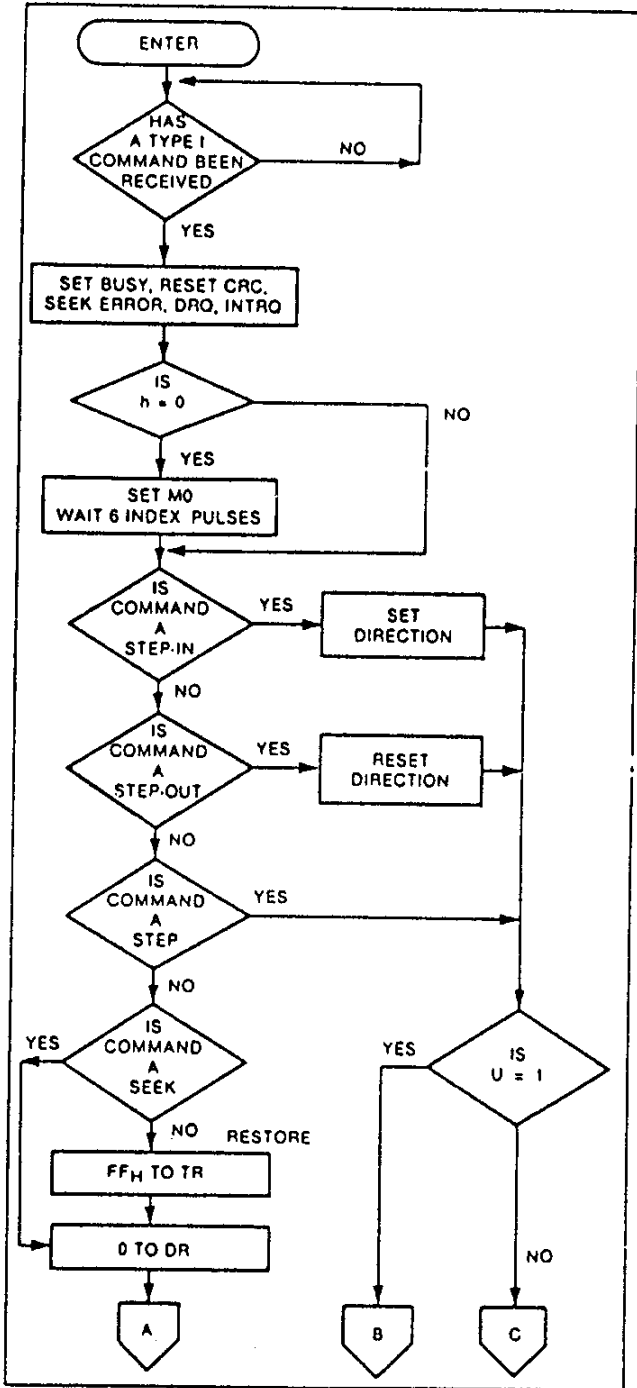
TYPE I COMMAND FLOW
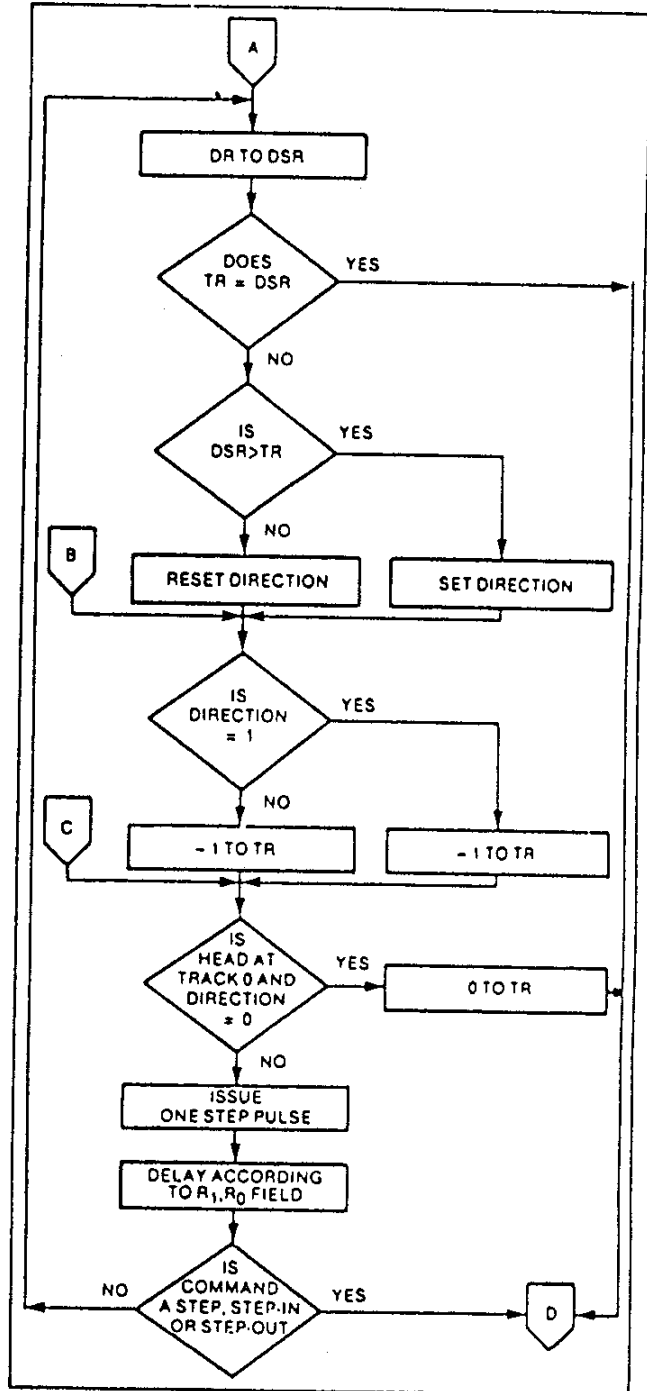
TYPE I COMMAND FLOW

is high, the command executes immediately, defeating the 6 revolution start up. This feature allows consecutive Read or Write commands without waiting for motor start up each time; the WD1770/2-00 assumes the spindle motor is up to speed.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If TR00 is not active low, stepping pulses at a rate specified by the r_1, r_0 field are issued until the TR00 input is activated.

At this time, the Track Register is loaded with zeroes and an interrupt is generated. If the TR00 input does not go active low after 255 stepping pulses, the WD177X-00 terminates operation, interrupts, and sets the Seek Error status bit, providing the V flag is set.

TYPE I COMMAND FLOW

A verification operation also takes place if the V flag is set. The h bit allows the Motor On option at the start of a command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD177X-00 updates the Track Register and issues stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the Motor On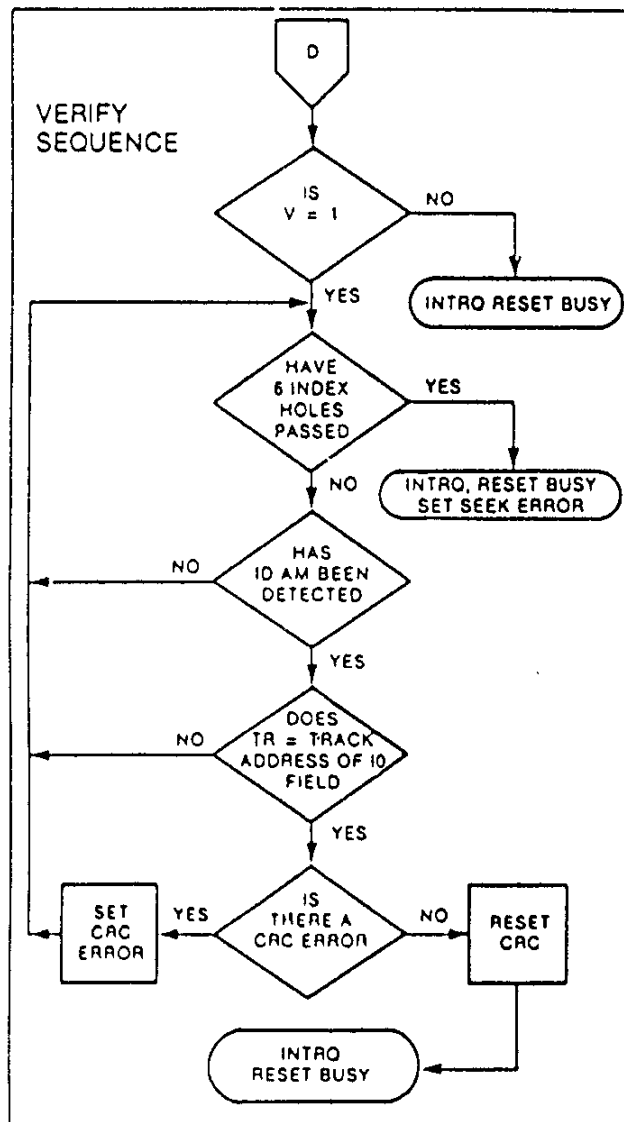 option at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the Track Register is updated for the drive selected before seeks are issued.

STEP

Upon receipt of this command, the WD177X-00 issues one Stepping Pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1, r_0 field, a verification takes place if the V flag is on. If the U flag is on, the Track Register is updated. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the WD177X-00 issues one Stepping Pulse in the direction towards track 76. If the U flag is on, the Track Register is incremented by one. After a delay determined by the r_1, r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the WD177X-00 issues one stepping pulse in the direction towards track 0. If the U flag is on, the Track Register is decremented by one. After delay determined by the r_1, r_0 field, a verification takes place if the V flag is on. The h bit allows the Motor On option at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer loads the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy Status bit is set. If the E flag = 1 the command executes after a 30 msec delay.

When an ID field is located on the disk, the WD177X-00 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sec-

TYPE II COMMAND

Each of the Type II Commands contains an m flag which determines if multiple records (sectors) are read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification occurs on the next record. The WD177X-00 continues to read or write multiple records and updates the Sector Register in numerical ascending sequence until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt Command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the WD177X-00 is instructed to read sector 27 and there are only 26 on the track, the Sector Register exceeds the number available. The WD177X-00 searches for 5 disk revolutions, interrupts out, resets Busy, and sets the Record Not Found Status Bit.

READ SECTOR

Upon receipt of the Read Sector Command, the Busy Status Bit is set, then when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field is found with 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte. If not, the ID field is searched for and verified again followed by the Data Address Mark search. If, after five revolutions the DAM is not found, the Record Not Found Status Bit is set and the operation is terminated. When the first character or byte of the data field is shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status Bit is set. This sequence continues until the complete data field is inputted to the computer. If there is a CRC error at the end of the data field, the CRC Error Status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector Command, the Busy Status Bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The WD177X-00 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the WG

tor Number of the ID field is compared with the Sector Register. If there is no Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is located and is either written into, or read from, depending upon the command. The WD177X-00 finds an ID field with a Track number, Sector number, and CRC within four revolutions of the disk, or, the Record Not Found Status bit is set (Status Bit 4) and the command is terminated with an INTRQ.

TYPE II COMMAND

output is made active if the DRQ is serviced (i.e., the DR is loaded by the computer). If DRQ is not serviced, the command is terminated and the Lost Data Status Bit is set. If the DRQ is serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are written on the disk. The Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown:

a_0	DATA ADDRESS MARK (BIT 0)
1	Deleted Data Mark
0	Data Mark

The WD177X-00 writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status

READ SECTOR
SEQUENCE
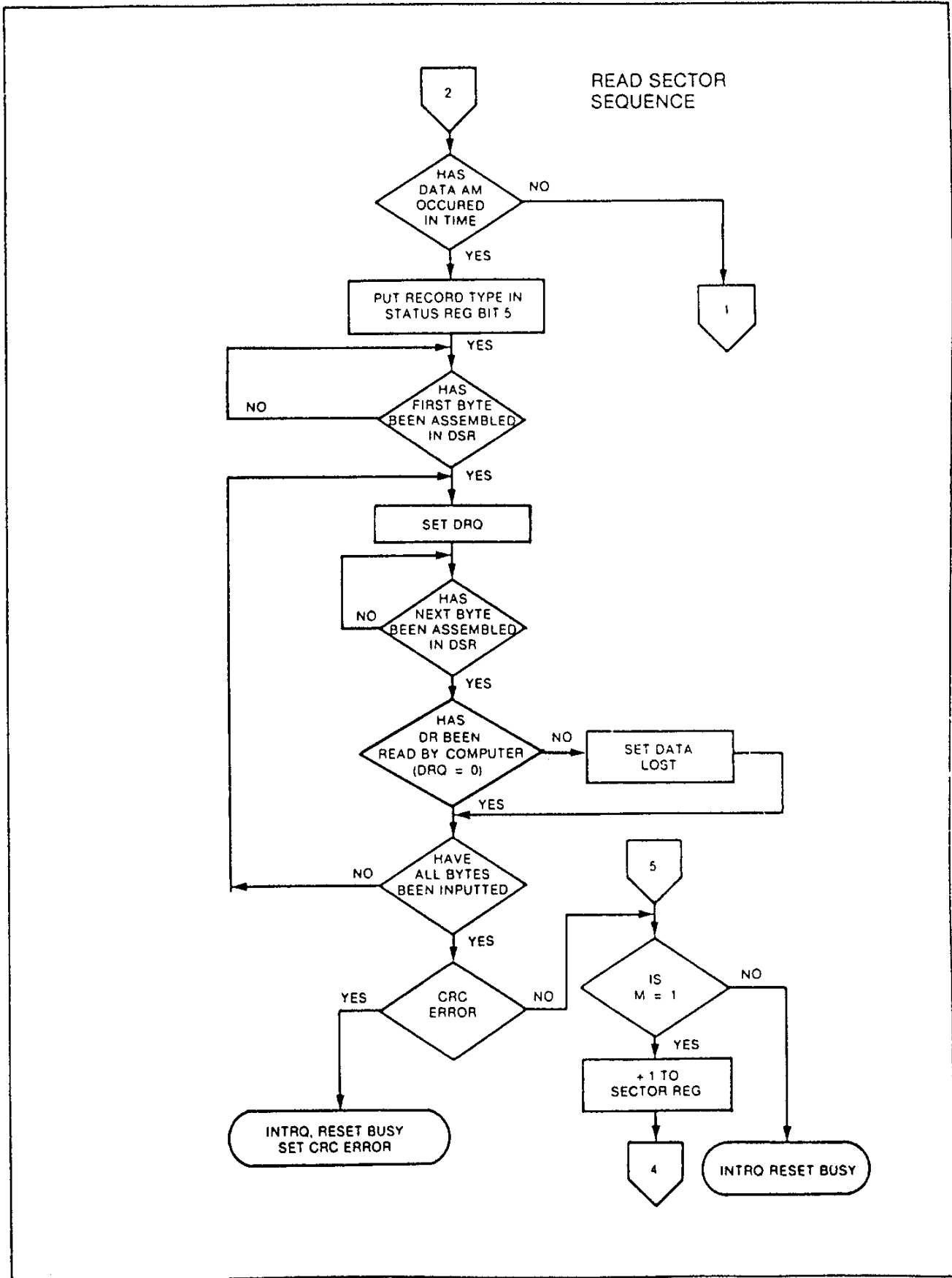
TYPE II COMMAND

SEQUENCE

```
                    ┌───┐
                    │ 3 │
                    └─┬─┘
                      ▼
          ┌───────────────────────┐
          │  DELAY 2 BYTES OF GAP │
          └───────────┬───────────┘
                      ▼
          ┌───────────────────────┐
          │        SET DRQ        │
          └───────────┬───────────┘
                      ▼
          ┌───────────────────────┐
          │  DELAY 9 BYTES OF GAP │
          └───────────┬───────────┘
                      ▼
                  HAS DR BEEN
             LOADED BY COMPUTER ──── NO ────►  INTRQ, RESET BUSY
                  (DRQ = 0)                       SET LOST DATA
                      │
                     YES
                      ▼
          ┌───────────────────────┐                    ┌──────────┐
          │  DELAY 1 BYTE OF GAP  │───────────────────►│  DDEN    │
          └───────────┬───────────┘                    │   = 0    │
                      │                          NO ◄───┤          ├──── YES
                      │                                 └──────────┘        │
                      ▼                                                     ▼
          ┌───────────────────────┐              ┌──────────────────────┐
          │   TURN ON WG & WRITE  │◄─────────────│    DELAY 11 BYTES    │
          │    6 BYTES OF ZEROES  │              └──────────┬───────────┘
          └───────────┬───────────┘                         ▼
                      ▼                          ┌──────────────────────┐
          ┌───────────────────────┐              │   TURN ON WG & WRITE │
          │     WRITE DATA AM     │◄─────────────│   12 BYTES OF ZEROES │
          │  ACCORDING TO A0 FIELD│              └──────────────────────┘
          │   OF WRITE COMMAND    │
          └───────────┬───────────┘
                      ▼
          ┌───────────────────────┐
          │   DR TO DSR, SET DRQ  │
          └───────────┬───────────┘
                      ▼
          ┌───────────────────────┐
          │   WRITE BYTE TO DISK  │
          └───────────┬───────────┘
                      ▼
                  HAS DR BEEN
                   LOADED ──── NO ────►   SET DATA LOST
                  (DRQ = 0)                WRITE BYTE
                      │                    OF ZEROES
                     YES
                      ▼
                    HAVE
                ALL BYTES ──── YES ────►   WRITE CRC
             ◄── BEEN WRITTEN                  │
               NO                              ▼
                                          WRITE 1 BYTE OF FF
                                              │
                                              ▼
                                          TURN OFF WG
                                              │
                                              ▼
                                           ┌───┐
                                           │ 5 │
                                           └───┘
```

TYPE II COMMAND

Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte is written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. INTRQ sets 24 μsec (MFM) after the last CRC byte is written. For partial sector writing, the proper method is to write data and fill the balance with zeroes.

TYPE III COMMANDS

Read Address
Upon receipt of the Read Address Command, the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown:

TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the WD177X-00 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the user. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track Command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQ's are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; and the Address Mark Detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM.

The ID AM, ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector are correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

WRITE TRACK FORMATTING THE DISK

(Refer to section on TYPE III commands for flow diagrams.)

Data and gap information are provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track Command.

Upon receipt of the Write Track Command, the Busy Status Bit is set. Writing starts with the leading edge of the first encountered Index Pulse and continues until the next Index Pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing does not start until after the first byte is loaded into the Data Register. If the DR is not loaded within three byte times, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.
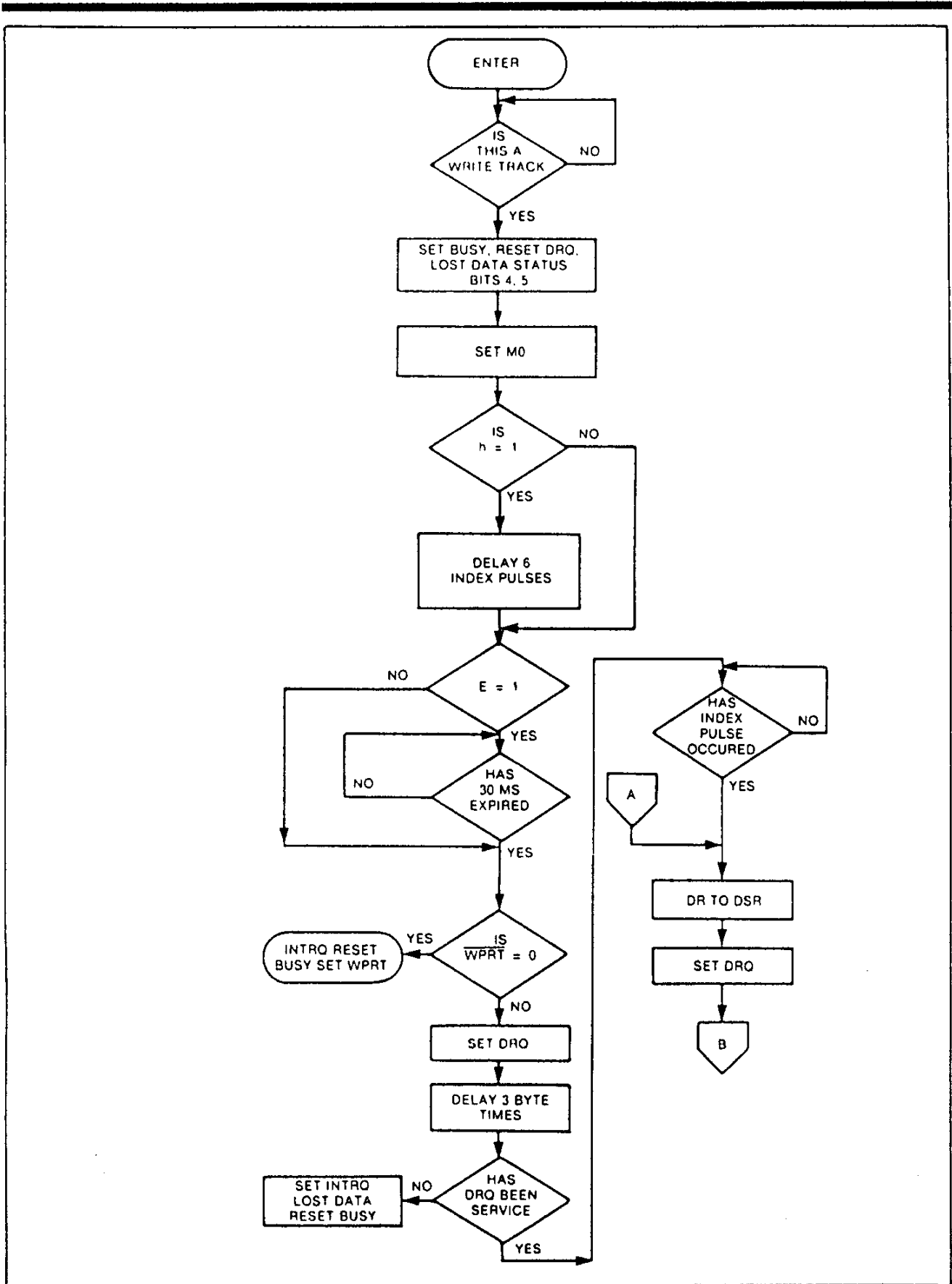
This sequence continues from one Index Pulse to the next. Normally whatever data pattern appears in the Data Register is written on the disk with a normal clock pattern. However, if the WD177X-00 detects a data pattern of F5 through FE in the Data Register, this is interpreted as Data Address Marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is transferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE do not appear in the gaps, data field, or ID fields. Also, CRC's are generated by an F7 pattern.

Disks are formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

DATA PATTERN IN DR (HEX)	IN FM (DDEN = 1)	IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Present CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5.
**Missing clock transition between bits 3 and 4.

ENTER

IS THIS A WRITE TRACK — NO

YES

SET BUSY, RESET DRQ, LOST DATA STATUS BITS 4, 5

SET M0

IS h = 1 — NO

YES

DELAY 6 INDEX PULSES

E = 1 — NO

YES

HAS 30 MS EXPIRED — NO

YES

IS $\overline{WPRT}$ = 0 — YES — INTRQ RESET BUSY SET WPRT

NO

SET DRQ

DELAY 3 BYTE TIMES

HAS DRQ BEEN SERVICE — NO — SET INTRQ LOST DATA RESET BUSY

YES

HAS INDEX PULSE OCCURED — NO

A

YES

DR TO DSR

SET DRQ

B

TYPE III COMMAND WRITE TRACK

B

DDEN = 0

YES (MFM)

NO (FM)

DOES DSR = F7 — YES → WRITE 2 CRC CHARS. CLK = FF

NO

DOES DSR = FC — YES → WRITE FC CLK = D7

NO

DOES DSR = FD, FE, OR F8-FB — YES → WRITE FD, FE OR F8-F9, CLK = C7 INITIALIZE CRC

NO

WRITE DSR CLK = FF

INTRQ RESET BUSY ← YES — PHYS INDEX MARK

NO

HAS DR BEEN LOADED — NO → WRITE BYTE OF ZEROES SET DATA LOST

YES

A

DOES DSR = F5 — YES → WRITE A1 IN MFM WITH MISSING CLOCK INITIALIZE CRC

NO

DOES DSR = F6 — YES → WRITE C2 IN MFM WITH MISSING CLOCK

NO

DOES DSR = FF — YES → WRITE 2 CRC CHARS.

NO

WRITE DSR IN MFM

TYPE III COMMAND WRITE TRACK

TYPE IV COMMANDS

The Forced Interrupt Command is used to terminate a multiple sector read or write command or to insure Type I status in the Status Register. This command is loaded into the Command Register at any time. If there is a current command under execution (Busy Status Bit set) the command is terminated and the Busy Status Bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not used (WD1770-00, WD1772-00), Not Ready To Ready Transition (WD1773-00)

I_1 = Not Used (WD1770-00, WD1772-00), Ready To Not Ready Transition (WD1773-00)

I_2 = Every Index Pulse

I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. When the condition for interrupt is met the INTRQ line goes high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (Hex D0), no interrupt occurs but any command presently under execution is immediately terminated. When using the immediate interrupt condition (I_3 = 1) an interrupt is immediately generated and the current command terminated. Reading the status or writing to the Command Register does not automatically clear the interrupt. The Hex D0 is the only command that enables the immediate interrupt (Hex D8) to clear on a subsequent load Command Register or Read Status Register operation. Follow a Hex D8 with D0 command.

Wait 16 μsec (double density) or 32 μsec (single density) before issuing a new command after issuing a forced interrupt. Loading a new command sooner than this nullifies the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt waits until ALU operations in progress are complete (CRC calculations, compares, etc.).

Status Register

Upon receipt of any command, except the Force Interrupt Command, the Busy Status Bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy Status Bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt Command is received when there is not a current command under execution, the Busy Status Bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQ's to reset.

The Busy Bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a Busy Status check is not recommended because a read of the Status Register to determine the condition of busy resets the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Because of internal sync cycles, certain time delays are observed when operating under programmed I/O, as shown.

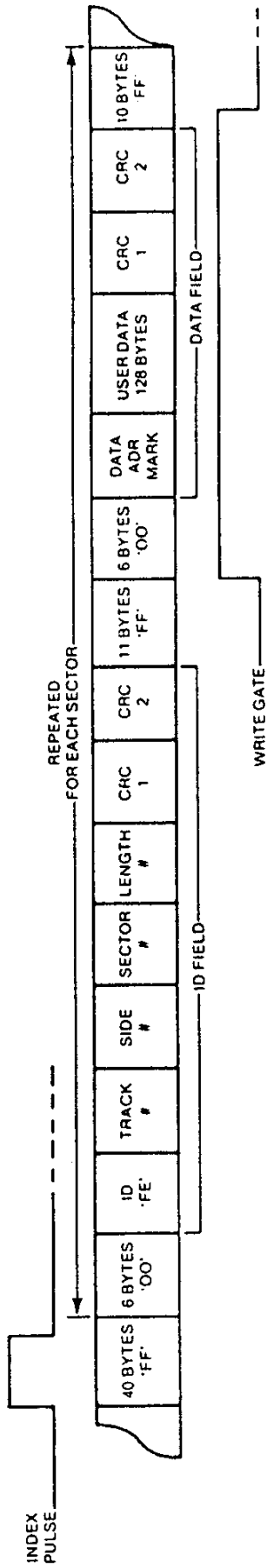| Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	48μsec	24μsec
Write to Command Reg.	Read Status Bits 1-7	64μsec	32μsec
Write Register	Read Same Register	32μsec	16μsec

RECOMMENDED - 128 BYTES/SECTOR

The recommended single-density format with 128 bytes/sector is shown. In order to format a diskette, the user issues the Write Track Command, and loads the Data Register with the following values. For every byte to be written, there is one Data Request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 10)
1	00 (Sector Length)
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or 00)
369**	FF (or 00)

*Write bracketed field 16 times.

**Continue writing until WD177X-00 interrupts out. Approx. 369 bytes.

SINGLE DENSITY FORMAT

INDEX PULSE

REPEATED FOR EACH SECTOR

| 40 BYTES 'FF' | 6 BYTES '00' | ID 'FE' | TRACK # | SIDE # | SECTOR # | LENGTH # | CRC 1 | CRC 2 | 11 BYTES 'FF' | 6 BYTES '00' | DATA ADR MARK | USER DATA 128 BYTES | CRC 1 | CRC 2 | 10 BYTES 'FF' |

ID FIELD

DATA FIELD

WRITE GATE

DOUBLE DENSITY FORMAT

INDEX PULSE

REPEATED FOR EACH SECTOR

| 60 BYTES '4E' | 12 BYTES '00' | 3 BYTES 'A1' | ID 'FE' | TRACK # | SIDE # | SECTOR # | LENGTH # | CRC 1 | CRC 2 | 22 BYTES '4E' | 12 BYTES '00' | 3 BYTES 'A1' | ID 'FB' | USER DATA 256 BYTES | CRC 1 | CRC 2 | 24 BYTES '4E' |

ID FIELD

DATA FIELD

WRITE GATE

256 BYTES/SECTOR

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user issues the Write Track Command and loads the Data Register with the following values. For every byte to be written, there is one data request.
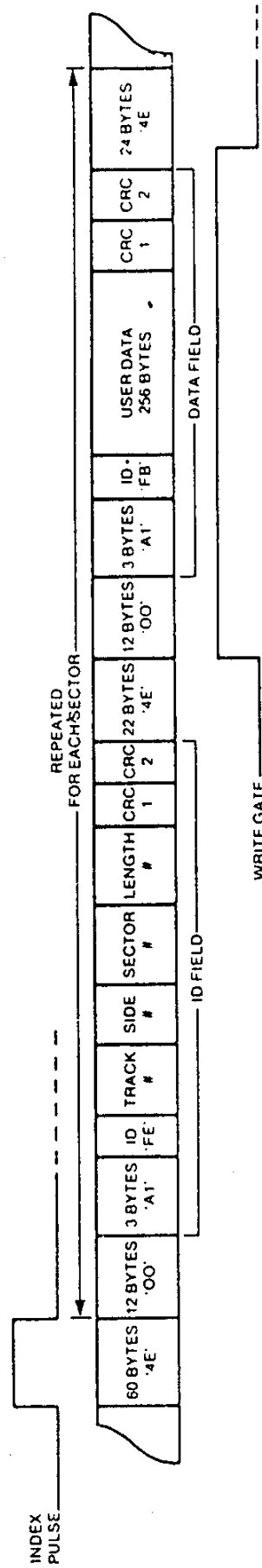
NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
60	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 10)
1	01 (Sector Length)
1	F7 (2 CRC's written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (Data Address Mark)
24	4E
668**	4E

*Write bracketed field 16 times.
**Continue Writing until WD177X-00 interrupts out. Approx. 668 bytes.

1. Non-Standard Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:
1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the WD177X-00. Gap 1, 3 and 4 lengths are as short as 2 bytes for WD177X-00 operation, however PLL lock up time, motor speed variation, write-splice area, etc. adds more bytes to each gap to achieve proper operation. For highest system reliability use the recommended format.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
*		3 bytes A1
Gap III**	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

STATUS REGISTER DESCRIPTION (WD1770-00 and WD1772-00 only)

BIT NAME	MEANING
S7 MOTOR ON	This bit reflects the status of the Motor On output.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/SPIN-UP	When set, this bit indicates that the Motor Spin-Up sequence has completed (6 revolutions) on Type I commands. Type 2 & 3 commands, this bit indicates record Type. 0 = Data Mark. 1 = Deleted Data Mark.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error data field. This bit is reset when updated.
S2 LOST DATA/ BYTE	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. On Type I commands, this bit reflects the status of the TR00 signal.
S1 DATA REQUEST INDEX	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. On Type 1 commands, this bit indicates the status of the IP signal.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS (WD1773-00 only)

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ORed" with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TR00 input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set, command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS (WD1773-00 ONLY)

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ORed" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desire track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

DC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Storage Temperature .... 55°C (67°F) to + 125°C (257°F)

Operating Temperature .... 0°C (32°F) to 70°C (158°F) Ambient

Maximum Voltage to Any Input with Respect to V_{SS} .... + 7V to -0.5V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC OPERATING CHARACTERISTICS

TA = 0°C(32°F) to 70°C (158°F), V_{SS} = OV, V_{CC} = +5V ± .25V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{CC}$
V_{IH}	Input High Voltage	2.0		V	
V_{IH}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	$I_0 = -100$ μA
V_{OL}	Output Low Voltage		0.40	V	$I_0 = 1.6$ mA
P_D	Power Dissipation		.75	W	
R_{PU}	Internal Pull-Up	100	1700	μA	$V_{IN} = 0V$
I_{CC}	Supply Current	75(Typ)	150	mA	

AC TIMING CHARACTERISTICS

TA = 0°C (32°F) to 70°C (158°F), V_{SS} = OV, V_{CC} = +5V ± .25V
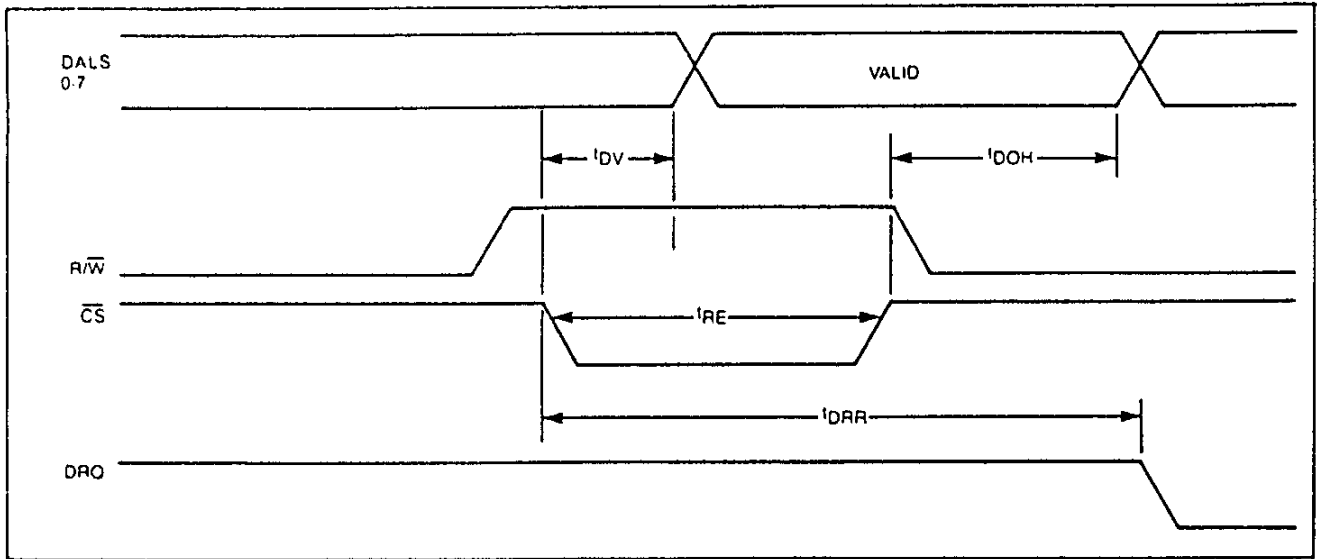
READ ENABLE TIMING

READ ENABLE TIMING – $\overline{RE}$ such that: R/$\overline{W}$ = 1, CS = 0.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{RE}	$\overline{RE}$ Pulse Width of $\overline{CS}$	200			nsec	$C_L = 50$ pf
t_{DRR}	DRQ Reset from $\overline{RE}$		200	300	nsec	
t_{DV}	Data Valid from $\overline{RE}$		100	200	nsec	$C_L = 50$ pf
t_{DOH}	Data Hold from RE	20		150	nsec	$C_L = 50$ pf
	INTRQ Reset from $\overline{RE}$			8	μsec	

Note: DRQ and INTRQ reset are from rising edge (lagging) of $\overline{RE}$, whereas resets are from falling edge (leading) of $\overline{WE}$. Worst case service time for DRQ is 23.5 μsec for MFM and 47.5 μsec for FM.
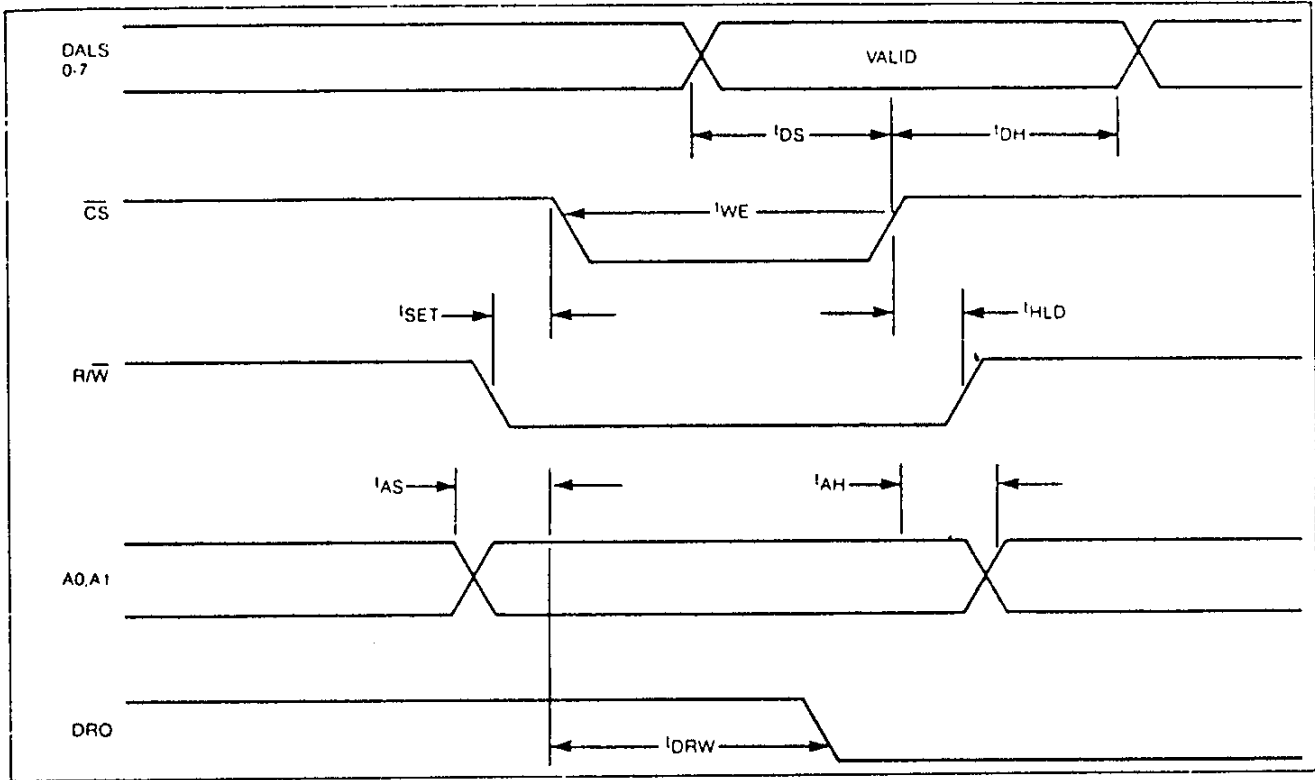
WRITE ENABLE TIMING

WRITE ENABLE TIMING – $\overline{WE}$ such that: $R/\overline{W} = 0$, $\overline{CS} = 0$.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{AS}	Setup ADDR to $\overline{CS}$	50			nsec	
t_{SET}	Setup $R/\overline{W}$ to $\overline{CS}$	0			nsec	
t_{AH}	Hold ADDR from $\overline{CS}$	10			nsec	
t_{HLD}	Hold $R/\overline{W}$ from $\overline{CS}$	0			nsec	
t_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
t_{DRW}	DRQ Reset from $\overline{WE}$		100	200	nsec	
t_{DS}	Data Setup to $\overline{WE}$	150			nsec	
t_{DH}	Data Hold from $\overline{WE}$	0			nsec	
	INTRQ Reset from $\overline{WE}$			8	μsec	

READ DATA TIMING:

CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{\text{Raw Read}}$ Pulse Width	.200		3	μsec	MFM
	.400		3		FM
$\overline{\text{Raw Read}}$ Cycle Time	3			μsec	

WRITE DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
	Write Gate to Write Data		4		μsec	FM
			2		μsec	MFM
	Write Data Cycle Time		4,6,8		μsec	
	Write Gate off from WD		4		μsec	FM
			2		μsec	MFM
t_{WP}	Write Data Pulse Width		820		nsec	Early MFM
			690		nsec	Nominal MFM
			570		nsec	Late MFM
			1.38		μsec	FM
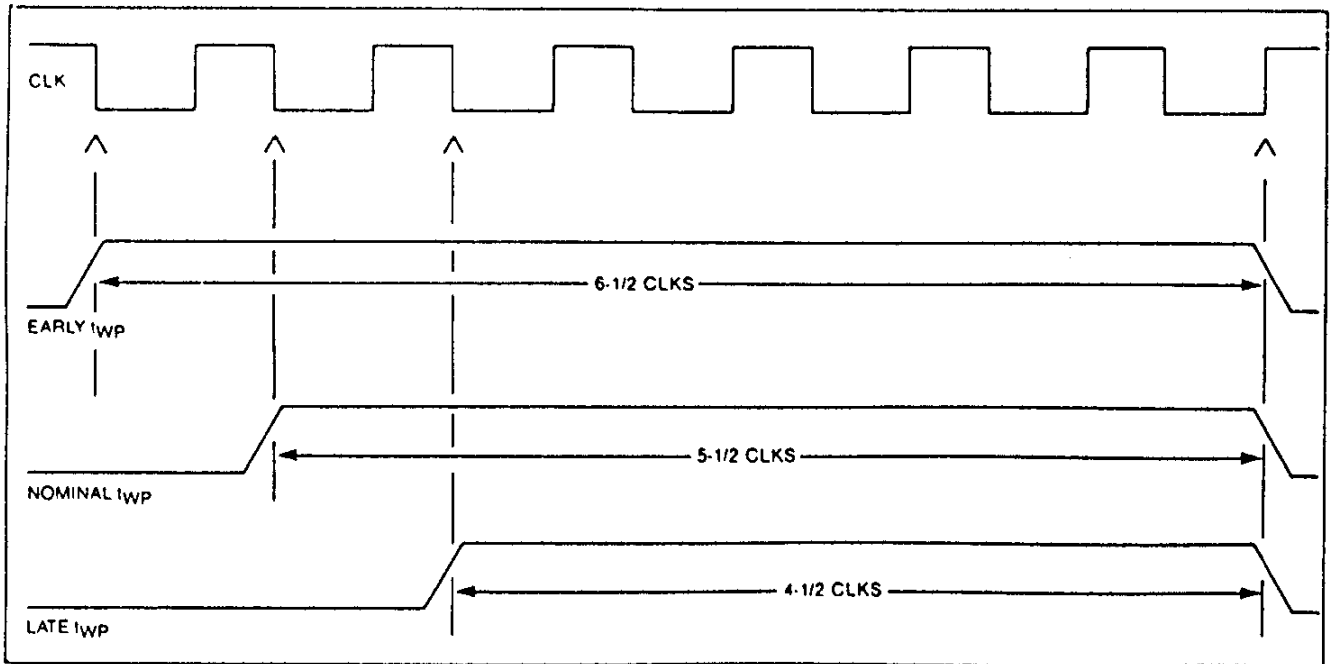
WRITE DATA TIMING
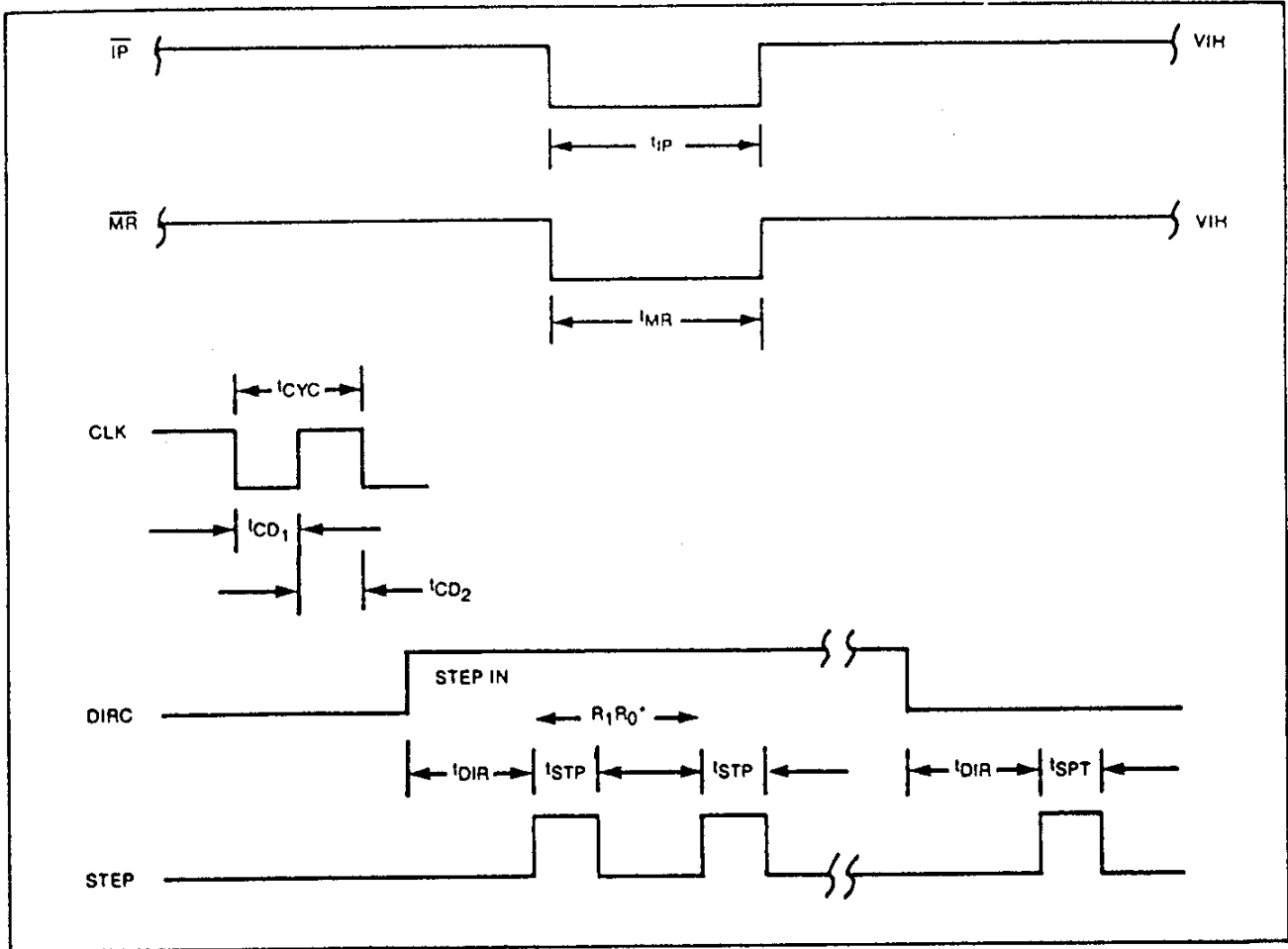
MISCELLANEOUS TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
t_{CD1}	Clock Duty (low)	50	67		nsec	
t_{CD2}	CLock Duty (high)	50	67		nsec	
t_{STP}	Step Pulse Output		4		μsec	MFM
			8			FM
t_{DIR}	Dir Setup to Step		24		μsec	MFM
			48			FM
t_{MR}	Master Reset Pulse Width	50			μsec	
t_{IP}	Index Pulse Width	20			μsec	