Ultimate1MB expansion features

Ultimate1MB expansion was designed with few things in my mind:

- to be as much solderless as possible (only RW, PHI2, HALT and RESET lines need soldering)
- fully flashable SpartaDOS-X with up to 432kbytes for its purposes
- RTC module for SDX with battery backup and NVRAM
- fully flashable 4 OS ROM slots
- hardware WRITE PROTECT for whole Flash array
- configurable memory expansion with 4 modes of operation:
    - disabled - no extra memory is visible to the system
    - 320k RAMBO - 256k of extra memory is visible both to CPU and ANTIC chips
    - 578k COMPY SHOP - 512k of extra memory is visible to CPU and ANTIC chip, bit 4 and 5 works in 130XE compatibility mode
    - 1088k RAMBO - 1MB of extra memory is visible to CPU and ANTIC chips
- customizable BASIC and MISSLE COMMAND slots (also flashable)
- System select/Memory exp mode select switch connector that can be overridden by software

How it works?

Since solderless approach was the main driving force behind this, some portions of PIA and GTIA chips had to be simulated within the CPLD chip.

When PORTB write is detected, hardware checks if internal shadow of PBCTL (D303) allows writes, and if so, value from Data bus is written to PORTB shadow. In the parallel, last value of PORTB shadow registers is stored into internal MMU CONTROL register to preserve current status of system rom, basic, self-test and missile command rom chips mappings, thus allowing flawless access to whole extended memory array.

Since there is internal SDX module care had to be taken for GTIA TRIG3 register.

Normally RD5 line from cartridge port is connected both to MMU chip and GTIA TRIG3 lines and since the goal was to incorporate this extension without the need of cutting any traces on motherboard, this register had to be shadowed (OS checks for TRIG3 status on every NMI, if there is a change on state of this line, OS assumes that cartridge was put in/removed and to prevent failures goes into endless loop).
With this shadow of TRIG3 register system can be fooled, and enabling or disabling "external" (to SDX module) cartridges can be done.

Lastly, there is configuration register which is used for configuring the extension according to configuration data stored in NVRAM - user can choose which OS ROM should be booted on power-on, what memory size machine should have and if SDX and RTC modules should be enabled.

Registers description

D301 PORTBS (WO)

Bits are mapped according to Atari mappings

D303 PBCTLS (WO)

Bit 2 - if set to zero, PORTB writes are disabled, also at D380 UCTL register is enabled, also physical PIA chip won't be read or written to at D380

D380 UCTL (WO)

Bits 1-0 - Memory expansion configuration mode

- 00 - Memory disabled
- 01 - 320k RAMBO
- 10 - 576k COMPY SHOP
- 11 - 1088K RAMBO

Bits 3-2 - System Select

- 00 - ROM Slot 1
- 01 - ROM Slot 2
- 10 - ROM Slot 3
- 11 - ROM Slot 4

Bit 4 - SDX disable, when set, SDX module is disabled

Bit 5 - RTC disable, when set, RTC module is disabled

Bit 6 - for future use, should be written 0

Bit 7 - OVERRIDE, when set, connector P4 status is discarded, and values from bits 0-3 are valid for system selection and memory expansion mode configuration

SDX Registers

D5E0 BANKNO (WO)

Bits 5-0	Bank number. Banks 0-53 are valid for SDX module. Bank 54 is BASIC ROM, bank 55 is MISSILE COMMAND or any other 8k game ROM image, banks 56-63 are for OS ROM slots. Access to all banks is provided through this port for flashing purposes
Bits 7-6	Reserved for future use, should be written 0

D5E1 SDXCTL (WO)

Bit 0	External Cartridge. When set (1), and bit 1 is set, external cartridge is OFF, SDX is OFF When reset (0), and bit 1 is set, external cartridge is ON, SDX is OFF
Bit 1	SDX Disable. When reset (0), SDX is ON, external cartridge is always OFF When set (1), SDX is OFF, external cartridge is controlled via bit 1
Bits 6-2	Reserved for future use, should be written 0
Bit 7	Reserved for future use, should be written 1

D5E2 RTCOUT (W)

Bit 0	Chip Enable
Bit 1	SPI Clock
Bit 2	SPI MOSI (Master Out, Slave In)
Bits 7-3	Reserved

D5E2 RTCIN (R)

Bit 0-2	Reserved
Bit 3	SPI MISO (Master In, Slave Out)
Bit 7-4	Reserved